SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

Approved by AICTE, Recognized by UGC & Affiliated to Anna University
Accredited by NBA-AICTE, NAAC-UGC with 'A+' Grade

Saravanampatti, Coimbatore -641035

CURRICULA AND SYLLABI

REGULATION 2019

CHOICE BASED CREDIT SYSTEM

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. – VLSI DESIGN

SNS COLLEGE OF TECHNOLOGY, Coimbatore-35.

(An Autonomous Institution)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REGULATION – 2019

SUGGESTED CURRICULUM AND SYLLABI I – IV SEMESTERS

M. E. VLSI DESIGN

SEMESTER I

S No.	Course Code	Course	L	T	P	J	Contact hrs/week	Credit	Int/Ext	Category
Theory Courses										
1.	19MAT605	Applied Mathematics for Electronics Engineers	3	1	0	0	4	4	50/50	FC
2.	19VLT601	Advanced Digital System Design	3	0	0	0	3	3	50/50	PC
3.	19VLT602	Computer Aided Design for VLSI	3	0	0	0	3	3	50/50	PC
4.	19VLT603	Digital CMOS VLSI Design	3	0	0	0	3	3	50/50	PC
5.	19VLT604	DSP Integrated Circuits	3	0	0	0	3	3	50/50	PC
6.		Professional Elective-I	3	0	0	0	3	3	50/50	PE
Theory Integrated Practical Courses										
7.	19GEB601	Design Thinking	2	0	0	2	4	3	60/40	EEC
Practical Courses										
8.	19VLP601	VLSI design- I Laboratory	0	0	4	0	4	2	50/50	PC
9.	19VLP602	Industrial Training I	0	0	0	4	4	2	100/0	EEC
	Total		**20**	**1**	**4**	**6**	**31**	**26**		

SEMESTER II										
S No.	**Course Code**	**Course**	**L**	**T**	**P**	**J**	**Contact hrs/week**	**Credit**	**Int/Ext**	**Category**
Theory Courses										
1.	19VLT605	Analog VLSI Design	3	0	0	0	3	3	50/50	PC
2.	19VLT606	Testing of VLSI Circuits	3	0	0	0	3	3	50/50	PC
3.	19VLT607	VLSI Signal Processing	3	0	0	0	3	3	50/50	PC
4.		Professional Elective-II	3	0	0	0	3	3	50/50	PE
5.		Professional Elective-III	3	0	0	0	3	3	50/50	PE
6.	19VLA751	Life skill course-I Professional Communication, Networking and Socialization	0	0	0	0	0	0	50/50	EEC
7.	19GET601	Career course-I Professional Development	2	0	0	0	2	2	50/50	EEC
Practical Courses										
8.	19VLP603	VLSI design-II Laboratory	0	0	4	0	4	2	50/50	PC
	Total		**17**	**0**	**4**	**0**	**21**	**19**		

SEMESTER III										
S No.	**Course Code**	**Course**	**L**	**T**	**P**	**J**	**Contact hrs/week**	**Credit**	**Int/Ext**	**Category**
Theory Courses										
1.		Professional Elective-IV	3	0	0	0	3	3	50/50	PE
2.		Open Elective	3	0	0	0	3	3	50/50	OE
3.	19GET602	Career Course II - Quality Assurance & Accreditation in Engineering Education	2	0	0	0	2	2	50/50	EEC

Practical Courses										
4.	19VLP701	Project Work Phase-I	0	0	0	20	20	10	50/50	EEC
	Total		**8**	**0**	**0**	**20**	**28**	**18**		

SEMESTER IV										
S No.	**Course Code**	**Course**	**L**	**T**	**P**	**J**	**Contact hrs/week**	**Credit**	**Int/Ext**	**Category**
Practical Courses										
1.	19VLP702	Project Work Phase -II	0	0	0	24	24	12	50/50	EEC
	Total		0	0	0	24	24	12		

TOTAL CREDITS OF THE PROGRAMME : 75

FOUNDATION COURSE (FC)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	J	C
1.	19MAT605	Applied Mathematics for Electronics Engineers	4	3	1	0	0	4
		TOTAL	3	1	0	0	4	

PROFESSIONAL CORE (PC)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	J	C
1.	19VLT601	Advanced Digital System Design	3	3	0	0	0	3
2.	19VLT602	Computer Aided Design for VLSI	3	3	0	0	0	3
3	19VLT603	Digital CMOS VLSI Design	3	3	0	0	0	3
4	19VLT604	DSP Integrated Circuits	3	3	0	0	0	3
5	19VLT605	Analog VLSI Design	3	3	0	0	0	3

6	19VLT606	Testing of VLSI Circuits	3	3	0	0	0	3
7	19VLT607	VLSI Signal Processing	3	3	0	0	0	3
8	19VLP601	VLSI design- I Laboratory	2	0	0	4	0	2
9	19VLP603	VLSI design- II Laboratory	4	0	0	4	0	2
			TOTAL	21	0	8	0	25

PROFESSIONAL ELECTIVES (PE)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	J	C
1.	19VLE601	Device Modeling	3	3	0	0	0	3
2.	19VLE602	Hardware Description Language	3	3	0	0	0	3
3.	19VLE603	System on chip	3	3	0	0	0	3
4.	19VLE604	VLSI technology	3	3	0	0	0	3
5.	19VLE605	DSP Processors Architecture and Programming	3	3	0	0	0	3
6.	19VLE606	Physical Design Of VLSI circuits	3	3	0	0	0	3
7.	19VLE607	Analysis and Design of Analog Integrated Circuits	3	3	0	0	0	3
8.	19VLE608	Signal integrity for high speed devices	3	3	0	0	0	3
9.	19VLE609	ASIC and FPGA Design	3	3	0	0	0	3
10.	19VLE610	Digital VLSI Design	3	3	0	0	0	3
11.	19VLE611	CMOS Mixed Signal Circuit Design	3	3	0	0	0	3
12.	19VLE612	RF VLSI Design	3	3	0	0	0	3
13.	19VLE701	Designing with CPLD and FPGA	3	3	0	0	0	3
14.	19VLE702	Embedded System Design	3	3	0	0	0	3

15.	19VLE703	VLSI Architecture for Image and Video Processing	3	3	0	0	0	3
16.	19VLE704	Reconfigurable computing	3	3	0	0	0	3
17.	19VLE705	IP based VLSI Design	3	3	0	0	0	3
18.	19VLE706	Security solutions in VLSI	3	3	0	0	0	3
19.	19VLE707	Power Efficient VLSI Design	3	3	0	0	0	3
20.	19VLE708	Nanotechnology	3	3	0	0	0	3
21.	19VLE709	Network on Chip	3	3	0	0	0	3
22.	19VLE710	Scripting Languages for VLSI	3	3	0	0	0	3
		TOTAL	12	12	0	0	0	12

EMPLOYMENT ENHANCEMENT COURSES

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	J	C
1	19VLP602	Industrial Training I	2	0	0	0	4	2
2	19GEB601	Design Thinking	4	2	0	0	2	3
2	19VLA751	Life skill course-I Professional Communication, Networking and Socialization	0	0	0	0	0	0
3	19GET601	Career course-I Professional Development	2	2	0	0	0	2
4	19GET602	Career Course II Quality Assurance & Accreditation in Engineering Education	2	2	0	0	0	2
5	19VLP701	Project Phase-I	20	0	0	0	20	10
6	19VLP702	Project Phase-II	24	0	0	0	24	12
			TOTAL	6	0	0	50	31

OPEN ELECTIVE OFFERED TO OTHER PG PROGRAMMES

S. NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
1.	19VLO701	MEMS and its Applications	3	3	0	0	3	-
2.	19VLO702	Bluetooth Technology	3	3	0	0	3	-
3.	19VLO703	Multi core processor and systems	3	3	0	0	3	-
4.	19VLO704	VLSI Design Techniques	3	3	0	0	3	-
5.	19VLO705	Internet of Things	3	3	0	0	3	-
		TOTAL	3	3	0	0	3	

S.No.	SUBJECT AREA	Credits Per Semester				Total Credits
		I	II	III	IV	
1	**FC**	4				4
2	**PC**	14	11			25
3	**PE**	3	6	3		12
4	**OE**			3		3
5	**EEC**	5	2	12	12	31
6	**MC**	0	0	-	-	0
	TOTAL	**26**	**19**	**18**	**12**	**75**

19MAT605	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS (M.E. VLSI)	L	T	P	J	C
		4	1	0	0	4

UNIT I FUZZY LOGIC **9+3**

Classical logic – Multi valued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II MATRIX THEORY **9+3**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition – Toeplitz matrices and some applications.

UNIT III ONE DIMENSIONAL RANDOM VARIABLES **9+3**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a RandomVariable.

UNIT IV DYNAMIC PROGRAMMING **9+3**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V QUEUEING MODELS **9+3**

Poisson Process – Markovian queues – Single and Multi-server Models –Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

L : 45 T:15 P: 0 J: 0 Total: 60 PERIODS

REFERENCES

1. George.J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 2011.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2007.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers,8th Edition, Prentice – Hall of India, Private Ltd., New Delhi 2011.
4. Taha, H.A. Operations Research: An Introduction, Ninth Edition, Pearson Education Edition, Asia, New Delhi, 2011.
5. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 3rd edition, John Wiley and Sons, New York 2011.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Convert an Engineering statement problem into a mathematical probabilistic Statement.
CO2 Know how to compute certain matrix decompositions and some of their applications.
CO3 Calculate standard statistics from mass, distribution and density functions.
CO4 Recognize, interpret and apply a variety of random processes that occur in engineering.
CO5 Acquire adequate knowledge in the field of Fuzzy logic.

19VLT601 ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	J	C
3	0	0	0	3

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuit- design of iterative circuits-ASM chart and realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment- transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.

UNIT V SYSTEM DESIGN USING VHDL 9

VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Charles H.RothJr “Fundamentals of Logic Design” Thomson Learning 2005.
2 Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001.
3 ParagK.Lala “Fault Tolerant and Fault Testable Hardware Design” BS Publications,2002.
4 Parag K.Lala “Digital system Design using PLD” B S Publications,2003.
5 Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the concepts of sequential circuits and its modeling techniques
CO2 Analyze the asynchronous circuit design and types of hazards in circuit design
CO3 Familiarize the algorithmic methods used for fault diagnosing and testing in digital circuits
CO4 Infer the families of plds and its types with applications.
CO5 Apply the system design of digital circuits using VHDL programming.

19VLT602	COMPUTER AIDED DESIGN FOR VLSI	L	T	P	J	C
		3	0	0	0	3

UNIT I VLSI DESIGN METHODOLOGIES **9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES **9**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - Placement and Partitioning - Circuit representation - Placement algorithms – partitioning.

UNIT III FLOOR PLANNING **9**

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION **9**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS **9**

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley &Sons, 2002.

2 N.A. Sherwani, "Algorithms for VLSI Physical Design Automation",3rd edition.,2005, Springer International Edition.

3 Christophn Meinel& Thorsten Theobold, “Algorithm and Data Structures for VLSI Design”, KAP, 2002.

4 Rolf Drechsheler: “Evolutionary Algorithm for VLSI”, second edition.

5 Trim burger, “Introduction to CAD for VLSI”, Kluwer Academic Publisher, 2002.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the tools used for automation and graph theory in VLSI design methodologies
CO2 Infer the techniques used for placement and partitioning in VLSI circuit design
CO3 Illustrate the floor planning and routing algorithms in VLSI- CAD
CO4 Apply the simulation techniques in various levels of design abstraction
CO5 Analyze the types of synthesis tools used to schedule and assign the device modeling.

19VLT603	DIGITAL CMOS VLSI DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore"s constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulseand sense amplifier based Registers, Non-bistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters,Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES 9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models,Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Jan Rabaey, Anantha Chandrakasan, B Nikolic, 'Digital Integrated Circuits: ADesign Perspective'. Second Edition, Prentice Hall of India., 2009.

2 Jacob Baker, 'CMOS: Circuit Design, Layout, and Simulation', Third Edition, WileyIEEE Press, 2011

3 M J Smith, 'Application Specific Integrated Circuits', Addisson Wesley, 1997.

4 N.Weste, K. Eshraghian, 'Principles of CMOS VLSI Design'. Second Edition, Addision Wesley, 1993.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Familiarize the static and dynamic characteristic of MOSFET and its parameters.

CO2 Understand the concepts of combinational logic circuits with layout design rules

CO3 Analyze the sequential logic circuits and its clock and timing issues

CO4 Interpret the nature of datapath circuits in arithmetic circuits and memory devices

CO5 Estimate the clocking strategies used for designing synchronous circuit design

19VLT604	DSP INTEGRATED CIRCUITS	L	T	P	J	C
		3	0	0	0	3

UNIT I DSP INTEGARTED CIRCUITS AND VLSI CIRCUITTECHNOLOGIES **9**

Standard Digital Signal Processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II DIGITAL SIGNAL PROCESSING **9**

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS **9**

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES **9**

Multiprocessors and multicomputer, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN **9**

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processorand Interpolator as case studies.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.

2 Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach", Second Edition, Pearson Education, Asia.

3 KeshabK.Parhi, "VLSI Digital Signal Processing Systems design and Implementation",John Wiley & Sons, 1999.

4 Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the technologies used to design standard DSP processors

CO2 Identify the frequency response of DSP by types of Fourier transforms

CO3 Relate the characteristics of filters in DSP processors and its sampling factors

CO4 Synthesize the DSP architectures by means of various algorithmic techniques

CO5 Familiarize the various applications of arithmetic units and accumulator in DSP processors

19GEB601	DESIGN THINKING	L	T	P	J	C
	(Common to M.E CSE, ST, PSE, VLSI, TE)	1	0	0	4	3

UNIT I INTRODUCTION TO DESIGN THINKING 3+12

An brief insight to Design Thinking and Innovation- People Centered Design & Evoking the 'Right Problem'- Purpose of Design Thinking- Design Thinking Framework

UNITII PROCESS IN DESIGN THINKING (EMPATHY, DEFINE 3+12

Design Thinking Process – Empathy – Uncovering and Investigating Community Concerns - Define : Examine and Reflect on the problem - Reconsider and arrive at the right problem to solve - Research with the users and Context - Question Framing and Conducting Research - User Stories and Design Strategy

UNIT III CONCEPTING AND BUILDING (IDEA, CREATE) 3+12

Generating Ideas-Identifying top three ideas-Bundling the Ideas and create an concepts-Stories and Scenarios to that concepts-Rapid Prototyping

UNIT IV TESTING, REFINING AND PITCHING THE IDEAS 3+12

Importance of Testing with People-Testingour Design with People-Conducting the usability Test-Record Results, Enhance, Retest and Redefine Results-Creating a Pitch for our design.

UNIT V VALUE PROPOSITION DESIGN 3+12

Introduction-Key Partners- Key Activities- Key Resources- Value Propositions- Customer Relationship-Customer Segments- Channels- Cost Structure- Revenue Streams-Case study.

L :15 T: 0 P: 0 J: 60 T:75 PERIODS

REFERENCES

1 Idris Mootee, Design Thinking for Strategic Innovation - What They Can't Teach You at Business or Design School, 1st Edition, 2017, Wiley

2 Yves Pigneur, Greg Bernarda, Alan Smith, Trish Papadakos Alex Osterwalder, Value Proposition Design: How to Create Products and Services Customers Want, 2015, Wiley

3 Brown, Tim, and Barry Katz. Change by Design: How Design Thinking Transforms Organizations and Inspires Innovation, 2009, Harper Business.

COURSE OUTCOMES :

At the end of the course students should be able to

CO1 Able to empathize with a broad group of stakeholders to understand their needs through the ethnographic method.

CO2 Able to define and re-define innovation challenges by asking the right questions, and not necessarily focusing on the right answers.

CO3 Able to develop many creative ideas through structured brainstorming sessions

CO4 Able to develop rapid prototypes to bring their ideas into reality as quickly as possible, and obtain feedback.

CO5 Able develop visual literacy and articulacy to explain design decisions

19VLP601	VLSI DESIGN- I LABORATORY	L	T	P	J	C
		0	0	4	0	2

LIST OF EXPERIMENTS

1. Modeling of Combinational Digital system using VHDL.Solving problems using arrays
2. Modeling of Combinational Digital system using Verilog.
3. Modeling of Sequential Digital system using VHDL.
4. Modeling of Sequential Digital system using Verilog
5. Design and Implementation of ALU using FPGA
6. Simulation of NMOS and CMOS circuits using CADENCE
7. Implementation of MAC Unit using FPGA

MAJOR EQUIPMENTS / SOFTWARE REQUIRED

Hardware

- XILINX/ALTERA

Software

- Cadence/tanner/mentor graphics

L : 0 T: 0 P: 60 J: 0 Total:60 PERIODS

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the combinational circuits modeling in Verilog and VHDL
CO2 Understand the sequential circuits modeling in Verilog and VHDL
CO3 Design an ALU and implement by FPGA XILINX/ALTERA
CO4 simulate and analyze the transient response of NMOS and CMOS using CADENCE
CO5 Design a MAC and implement by FPGA XILINX/ALTERA

19VLP602	INDUSTRIAL TRAINING I	L	T	P	J	C
		-	-	-	4	2

Minimum of two weeks in an Industry in the area of Electronics and communication Engineering. The summer internship should give exposure to the practical aspects of the discipline. In addition, the student may also work on a specified task or project which may be assigned to him/her. The outcome of the internship should be presented in the form of a report.

Total :2 weeks

19VLT605	ANALOG VLSI DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT I ANALOG CIRCUIT BUILDING BLOCKS **9**

Switches, active resistors - Current sources and sinks - Current mirrors/amplifiers - Voltage and current references, Comparator, Multiplier.

UNIT II AMPLIFIERS **9**

MOS and BJT inverting amplifier - Improving performance of inverting amplifier - CMOS andBJT differential amplifiers - Characterization of Op-Amp - The BJT two stage op-amp - The CMOS two stage op-amp -Op-amps with output stage, Folded Cascode op-amp, Trans conductance Amplifier.

FILTERS

Low pass filters - High pass filters – Band Pass filters – Phase Locked Loops.

UNIT III DATA CONVERTER FUNDAMENTALS **9**

Ideal A/D and D/A converters, Quantization noise, Signed codes, Performance limitations

UNIT IV D/A AND A/D CONVERTERS **9**

D/A converter: Current scaling, Voltage scaling and Charge scaling D/A converters - Serial D/A converters - Serial A/D converters, Parallel - High performance A/D converters

UNIT V LAYOUT ISSUES **9**

CMOS design rules - layout of CMOS - BJT- Capacitors – Resistors - Mixed layout issues: Floor planning, power supply & ground, fully differential matching, Guard rings and shielding.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Randall L Geiger, Phillip E Allen and Noel R Strader, "VLSI Design Techniques forAnalog and Digital Circuits", McGraw Hill, International Edition, 1990.

2 Jose E Franca HannisTsividis, “Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing”, Prentice Hall, International Edition, 2002.

3 David A Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 2002.

4 Phillip Allen and Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2000.

5 Benhard Razavi, “Data Converters”, Kluwer Publishers, 2000.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Familiarize the basic blocks of analog circuits and its applications

CO2 Understand the characteristics of amplifiers and filters used in analog circuits

CO3 Infer the fundamental design in data converters with its limitations

CO4 Analyze the performance of serial and parallel type data converters

CO5 Estimate the performance of Analog chip by CMOS layout design rules

19VLT606	TESTING OF VLSI CIRCUITS	L	T	P	J	C
		3	0	0	0	3

UNIT I BASICS OF TESTING AND FAULT MODELING 9

Introduction to testing – Faults in Digital Circuits – Modeling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Test generation for combinational logic circuits – Testable combinational logic circuit design –Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002

2 P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

3 M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002. [Unit I, II, III]

4 A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002. [Unit I,II]

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the basic concepts of fault modeling and detection in digital circuits

CO2 Familiarize the methods of test generation by combinational and sequential logic circuits

CO3 Infer the concept of DFT by various scan based approaches

CO4 Estimate the faulty circuits using BIST architectures by test algorithms

CO5 Analyze the digital circuits using logic and system level diagnostics

19VLT607	VLSI SIGNAL PROCESSING	L	T	P	J	C
		3	0	0	0	3

UNIT-I PIPELINING AND PARALLEL PROCESSING OF DIGITALFILTERS **9**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallelprocessing of FIR filters, Pipelining and Parallel processing for low power.

UNIT-II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE I **9**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT-III ALGORITHIMIC STRENGTH REDUCTION -II **9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT-IV BIT-LEVEL ARITHMETIC ARCHITECTURES **9**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT-V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING **9**

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled
data versus dual rail protocol.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.

2 U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Familiarize the pipelining an parallel processing of filters in VLSI circuits

CO2 Analyze the algorithmic strength reduction techniques in FIR filters

CO3 Analyze the algorithmic strength reduction techniques in IIR filters

CO4 Understand the basic concepts of bit level arithmetic architectures

CO5 Estimate the strength reduction, clocking and pipelining approaches in VLSI Processors

19VLA751	PROFESSIONAL COMMUNICATION, NETWORKING AND SOCIALIZATION	L	T	P	J	C
	(Common to M.E CSE & VLSI)	-	-	-	-	-

UNIT I

Neetisatakam-Holistic development of personality-Verses- 19,20,21,22(wisdom) -Verses- 29,31,32 (pride &heroism)-Verses- 26,28,63,65(virtue)-Verses- 52,53,59(dont's)-Verses- 71,73,75,78(do's)

UNITII

Approach to day to day work and duties-ShrimadBhagwadGeeta: Chapter 2-Verses 41, 47, 48- Chapter 3-Verses 13, 21, 27, 35,-Chapter 6-Verses 5, 13,17, 23,35-Chapter 18-Verses 45, 46,48.

UNIT III

Statements of basic knowledge-ShrimadBhagwadGeeta: Chapter2-Verses 56, 62,68-Chapter 12 - Verses 13, 14, 15, 16,17,18-Personality of Role model. ShrimadBhagwadGeeta: Chapter2-Verses 17,Chapter 3-Verses 36,37,42-Chapter 4-Verses 18,38,39-Chapter18Verses37,38,63

REFERENCES

1 "Srimad Bhagavad Gita" by Swami SwarupanandAadvaita Ashram (Publication Department),Kolk

2 Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriy Sanskrit Sansthanam, NewDelhi.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life

CO2 The person who has studied Geeta will lead the nation and mankind to peace and prosperity

CO3 Study of Neetishatakam will help in developing versatile personality of students.

19VLP603 **VLSI DESIGN- II LABORATORY**

L	T	P	J	C
0	0	4	0	2

LIST OF EXPERIMENTS

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD.
3. Design and Implementation of the following adders using FPGA
   - Ripple carry adder
   - Carry save adder
   - Carry look ahead adder
   - Carry bypass adder
   - Carry select adder
4. Design and Implementation of the following multiplier using FPGA.
   - Array multiplier
   - Booth multiplier
   - Wallace multiplier
   - Baugh wooley multiplier
5. Simulation of the following circuits using CADENCE
   - Transmission gate
   - Pass transistor logic(NAND,NOR)
   - Domino logic (NAND,NOR)
   - D latch
   - Current mirror
   - Differential pair
6. Design and Implementation of the following adders using CADENCE
   Full adder(8T,10T,12T,16T)

MAJOR EQUIPMENTS / SOFTWARE REQUIRED

Hardware

- XILINX/ALTERA

Software

- Cadence/tanner/mentor graphics

L : 0 T: 0 P: 60 J: 0 Total:60 PERIODS

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the concepts of ALU and Processorand design using XILINX/ALTERA
CO2 Design and implement the types of adders using FPGA
CO3 Design and implement the types of Multipliers using FPGA
CO4 Analyze and evaluate the performance of dynamic digital circuits using CADENCE
CO5 Evaluate the transient response of NMOS and CMOS level adders using CADENCE

19GET602	QUALITY ASSURANCE & ACCREDITATION IN ENGINEERING EDUCATION	L	T	P	J	C
	(Common to M.E CSE, ST, SW, PSE, VLSI, TE & M.Tech IT)	2	0	0	0	2

UNIT I CENTER FOR LEARNING AND TEACHING (CLT) 7

Learning Resources-Model & Mini project- Industry Specific Assignment - Industrial case study - MOOC-Teachers Manual-Workbook-LMS & Quality Assurance in Academic Performance-GATE.

UNIT II CENTRE FOR CREATIVITY (CFC) 6

Project-Product Development-Patent-Consultancy-Books/Book chapter- Research/Seminar Grant-Publications - Industry collaborated laboratories - Foreign collaboration & Exchange.

UNIT III SKILL AND CAREER DEPARTMENT (SCD) 5

Hackathon/Industrial contest- Project Proposal- Certification courses-Placement training-Schemes for student motivation-Clubs-Sports

UNIT IV SOCIAL RESPONSIBILITY INITIATIVE (SRI) 4

Need for outreach-Types of outreach –Stake holder communication-website-newsletter-magazine-meetings.

UNIT V INDUSTRY INSTITUTE PARTNERSHIP CELL (IIPC) 4

Industrial networking- MoU-Industrial delivery -workshop- Internship/Training-Partial delivery-Adjunct Professor- Placement- Campus companies-Start-Up.

UNIT VI INTERNAL QUALITY ASSURANCE CELL (IQAC) 4

Importance of IQAC- members- Goal setting-Audit-Feedback system-Governing bodies-Accreditation bodies - process-Ranking.

L :30 T: 0 P: 0 J: 0 T:30 PERIODS

REFERENCES

1. João Rosa, Maria, Amaral, A. (Eds.) “Quality Assurance in Higher Education “ Editors: Palgrave Macmillan publications, 2014.
2. Stuart Walesh,”Introduction to Creativity and Innovation for Engineers” , Pearson’s education, 2017.
3. Borich, “Effective Teaching Methods: Research-Based Practice”, Pearson education, 2016.

COURSE OUTCOMES :

At the end of the course students should be able to

CO1 Aware about the learning and teaching process.

CO2 Enrich their creative ability through research, product development, consultancy etc.

CO3 Know about the skills related to career development.

CO4 Understand the needs of societal responsibilities of an individual.

CO5 Collaborate industry institute partnership through various activities.

19VLP701	Project Work - Phase I	L	T	P	J	C
		0	0	0	20	10

1. Identification of a real life problem in thrust areas
2. Developing a mathematical model for solving the above problem
3. Finalization of system requirements and specification
4. Proposing different solutions for the problem based on literature survey
5. Future trends in providing alternate solutions
6. Consolidated report preparation of the above

L : 0 T: 0 P:0 J:300 Total: 300 PERIODS

19VLP702	PROJECT WORK PHASE – II	L	T	P	J	C
		0	0	0	24	12

The project involves the following:

Preparing a project - brief proposal including

1. Problem identification
2. A statement of system / process specifications proposed to be developed (block diagram / concept tree)
3. List of possible solutions including alternatives and constraints
4. Cost benefit analysis
5. Time line of activities

A report highlighting the design finalization [based on functional requirements & standards (if any)

A presentation including the following:

1. Implementation phase (hardware / software / both)
2. Testing & validation of the developed system
3. Learning in the Project
4. Consolidated report preparation

L: 0 T: 0 P: 0 J:360 TOTAL : 360 PERIODS

19VLE601	DEVICE MODELING	L	T	P	J	C
		3	0	0	0	3

UNIT-I SEMICONDUCTOR PHYSICS 9

Quantum Mechanical Concepts- Carrier Concentration- Transport Equation- Mobility and Resistivity- Carrier diffusion- Carrier Generation and Recombination- Continuity equation- Tunneling and High field effects- Ideal diode current equation.

UNIT-II DIODE MODELING 9

Static, Small signal and Large signal models of PN junction Diode-SPICE model for a Diode- Temperature and Area effects on Diode Model Parameters

UNIT-III BIPOLAR DEVICE MODELING 9

Transistor Action-Terminal currents - Switching- Static, Small signal and Large signal Eber- Moll models of BJT- Gummel Poon Model- SPICE modeling - temperature and area effects.

UNIT-IV MOSFET MODELING 9

MOS Transistor – NMOS- PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel and Narrow Width Effect- Models for Enhancement-Depletion Type MOSFET- MOS Models in SPICE.

UNIT-V OPTOELECTRONIC DEVICE MODELING 9

Static and Dynamic Models - Rate Equations - Numerical Technique - Equivalent Circuits - Modeling of LEDs - Laser Diode and Photo detectors.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 KiatSeng Yeo, Samir S.Rofail, Wang-Ling Gob, "CMOS / BiCMOS ULSI – LowVoltage, Low Power", Person education, Low price edition, 2003

2 Sze S.M. "Semiconductor Devices - Physics and Technology", John Wiley and sons,1985

3 Giuseppe Massobrio and Paolo Antogentti, "Semiconductor Device Modeling withSPICE" Second Edition, McGraw-Hill Inc, New York, 1993

4 Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", PearsonEducation ASIA, 2nd edition, 2000

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the basic concepts of quantum mechanics and its characteristics.

CO2 Develop a small and large signal model of diode and analyze its parameters

CO3 Analyze the channel effects of BJT with SPICE modeling

CO4 Analyze the channel effects of MOSFET with SPICE modeling

CO5 Design a static and dynamic model of optoelectronic devices.

19VLE602	HARDWARE DESCRIPTION LANGUAGE	L	T	P	J	C
		3	0	0	0	3

UNIT-I BASIC CONCEPTS OF HARDWARE DESCRIPTIONLANGUAGE **9**

Comparison between HDL and High Level Language Hierarchy, Concurrency, Logic and Delay Modeling, Structural, Data flow, Behavioral Styles of Hardware Description, Architecture of event driven simulation.

UNIT-II VHDL **9**

Data Types, Operators, Classes of Objects, entities and architectures , Attributes – concurrent statements- sequential statements- signals and variables- Behavior, dataflow and structural modeling- Configurations, functions- procedures- packages - test benches- Design Example

UNIT-III VERILOG **9**

Signals, Identifier Names, Net and Variable Types, operators, Gate instantiations, Verilog module, concurrent and procedural statements, UDP, sub circuit parameters, function and task, - test benches- Design Examples.

UNIT-IV TIMING ISSUES **9**

Modeling delay, Timing Modeling, Timing Assertion, Setup and hold times for clocked devices.

UNIT-V SYSTEM MODELLING **9**

Processor model, RAM model, UART Model, Interrupt Controller

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Bhasker J, “A VHDL Primer”, Prentice Hall, 1999
2 Michael D Ciletti, “Advanced Digital Design with Verilog HDL”, Pearson education,2005
3 Douglass Perry, “VHDL”, Tata McGraw Hill, McGraw-Hill Professional, 4th Edition,May 2002.[
4 Volnei A Pedroni, “Circuit Design with VHDL”, Prentice Hall, 2004
5 Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, PrenticeHall NJ, USA, 2003
6 Neil Weste and Kamran Eshranghian “Principles of CMOS VLSI Design”, Addison Wesley, 2000.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the fundamentals and various levels of abstractions in HDL
CO2 Familiarize the basic concepts of VHDL and test benches with design examples
CO3 Infer the basic concepts of Verilog and test benches with design examples
CO4 Analyze the timing issues of clocked devices in digital logic circuits.
CO5 Model a system using Verilog/VHDL and estimate its performance.

19VLE603	SYSTEM ON CHIP	L	T	P	J	C
		3	0	0	0	3

UNIT I INTRODUCTION TO PROCESSOR DESIGN 9

Abstraction in hardware design- MUO – a simple processor – Processor Design trade off- Design for low power consumption.

ARM ARCHITECTURE: Acorn RISC Machine – Architecture Inheritance – ARM Programming Model- ARM Development Tools – 3 and 5 Stage Pipeline ARM Organization -ARM Instruction Execution and Implementation – ARM Co-Processor Interface.

UNIT II ARM ASEEMBLY LANGUAGE PROGRAMMING 9

ARM Instruction Types – Data Transfer, Data Processing and Control Flow Instructions - ARM Instruction Set – Co-Processor Instructions.

UNIT III ARCHITECTURAL SUPPORT FOR HIGH LEVEL LANGAUGE 9

Data Types – Abstraction in software Design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory.

MEMORY HIERARCHY: Memory Size and Speed – On Chip Memory – Caches – Cache Design – an Example- Memory management.

UNIT IV ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT 9

Advanced Microcontroller Bus Architecture – ARM Memory Interface – ARM Reference Peripheral Specification – Hardware System Prototyping Tools – Armulator – Debug Architecture**.**

UNIT V ARCHITECTURAL SUPPORT FOR OPERTAING SYSTEM 9

An Introduction to Operating Systems – ARM System Control Coprocessor- CP15 Protection Unit Registers – ARM Protection Unit – CP15 MMU Registers – ARM MMU Architecture – Synchronization –Context Switching Input and Output.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Steve Furber, "ARM System on Chip Architecture", Addison- Wesley Professional, 2nd Edition, Aug 2000.

2 Ricardo Reis "Design of System on a Chip: Devices and Components" Springer, 1st Edition, July 2004

3 Jason Andrews "Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)" Newnes, BK and CD-ROM (Aug 2004).

4 Rashinkar P, Paterson and Singh L, "System on a Chip Verification – Methodologies and Techniques", Kluwer Academic Publishers, 2001

5 System on chip verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001 Kluwer Academic Publishers.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 understand the fundamental concepts of ARM architecture and its pipeliningapproach

CO2 Infer the types of instruction set in ARM processors and its co processors

CO3 Analyze the architectural support and memory hierarchy of ARM processors

CO4 Familiarize the concepts of advanced and reference microcontroller busarchitecture

CO5 Examine the ARM support architecture and its system control unit

19VLE604	VLSI TECHNOLOGY	L	T	P	J	C
		3	0	0	0	3

UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY ANDOXIDATION **9**

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems,Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING **9**

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments

UNIT III DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION **9**

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION **9**

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES **9**

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – packaging design consideration – VLSI assembly technology – Package fabrication technology

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 S.M.Sze, "VLSI Technology", Mc.Graw.Hill Second Edition. 2002.

2 Douglas A. Pucknell and Kamran Eshraghian, "Basic VLSI Design", Prentice HallIndia. 2003.

3 Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design", PrenticeHall India.2000.

4 Wayne Wolf,"Modern VLSI Design", Prentice Hall India.1998.

5 Essentials of VLSI circuits and Systems, K.Eshraghian ,Eshraghian.D, A.Pucknell,2005, PHI

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the techniques used for IC fabrication.

CO2 Infer the methods of etching and lithography for IC fabrication

CO3 Relate various methods of oxidation, diffusion and implantation techniques.

CO4 Apply the integration and simulation process of IC fabrication

CO5 Explain the assembly and packaging techniques in IC fabrication.

19VLE605	DSP PROCESSOR ARCHITECTURE ANDPROGRAMMING	L	T	P	J	C
		3	0	0	0	3

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs 9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs– Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II TMS320C5X PROCESSOR 9

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Simple programs-Application Programs for processing real time signals.

UNIT III TMS320C3X PROCESSOR 9

Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

UNIT IV ADSP PROCESSORS 9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V ADVANCED PROCESSORS 9

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture,Programming and Applications" – Tata McGraw – Hill Publishing Company Limited.New Delhi, 2003

2 User guides Texas Instrumentation, Analog Devices, Motorola.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the fundamental concepts of various programmable dsps.

CO2 Infer the characteristics and operations of TMS-5X processors.

CO3 Understand the functions and operations of TMS-3X processors.

CO4 Analyze the performance and characteristics of ADSP.

CO5 Compare the performance of various advanced DSP and applications.

19VLE606	PHYSICAL DESIGN OF VLSI CIRCUITS	L	T	P	J	C
		3	0	0	0	3

UNIT I INTRODUCTION TO VLSI TECHNOLOGY 9

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies-Packaging- Computational Complexity-Algorithmic Paradigms

UNIT II PLACEMENT USING TOP-DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic-Ratio cut-partition with capacity and i/o constraints. Floor planning: Rectangular dual floor planning-hierarchical approach- simulated annealing- Floor plan sizing.

Placement: Cost function- force directed method- placement by simulated annealing- partitioning placement- module placement on a resistive network – regular placement- linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches-hierarchical approaches- multi commodity flow based techniques- Randomized Routing- One Step approach- Integer Linear Programming .Detailed Routing: Channel Routing- Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs .

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization-
unconstrained via Minimization- Other issues in minimization.

UNIT V SINGLE LAYER ROUTING CELL GENERATION AND COMPACTION 9

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing-Multiple chip modules(MCM)- Programmable Logic Arrays- Transistor chaining- WeinBurger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw HillInternational Edition 1995.

2 Preas M. Lorenzatti, " Physical Design and Automation of VLSI systems", TheBenjamin Cummins Publishers, 1998.

3 Wayne Wolf, "Modern VLSI Design System – On-chip Design", Pearson Education FirstIndian Reprint 2002.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the basic concepts of gate array with algorithm paradigms

CO2
CO3 Infer the methods of placement and partitioning using various algorithms

CO4 Understand the fundamental routing techniques used in FPGA design

CO5 Estimate various performance metrics in FPGA circuit layout

Familiarize the concepts of circuit compaction in PLA

19VLE607	ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS	L	T	P	J	C
		3	0	0	0	3

UNIT-I SINGLE STAGE AMPLIFIERS 9

Common source stage- Source follower- Common gate stage-Cascode stage- Single ended and differential operation- Basic differential pair -Differential pair with MOS loads.

UNIT-II BIASING CIRCUITS 9

Basic current mirrors, cascode current mirrors, active current mirrors voltage references,supply independent biasing- temperature independent references-PTAT current generation- Constant-Gm Biasing.

UNIT-III FREQUENCY RESPONSE AND NOISE ANALYSIS 9

Miller effect, Association of poles with nodes-frequency response of common source stage- Source followers-Common gate stage, Cascode stage, Differential pair-Statistical characteristics of noise-, noise in single stage amplifiers, noise in differential amplifiers.

UNIT-IV OPERATIONAL AMPLIFIERS 9

Concept of negative feedback- Effect of loading in feedback networks operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps- Input range limitations- Gain boosting- slew rate power supply rejection- noise in Op Amps.

UNIT-V STABILITY AND FREQUENCY COMPENSATION 9

General considerations- Multipole systems - Phase Margin - Frequency Compensation- Compensation of two stage Op Amps- Slewing in two stage Op Amps- Other compensation techniques.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1. BehzadRazavi, ―Design of Analog CMOS Integrated Circuits‖, Tata McGraw Hill, 2001
2. Willey M.C. Sansen, ―Analog design essentials‖, Springer, 2006.
3. Grebene, ―Bipolar and MOS Analog Integrated circuit design‖, John Wiley &sons,Inc.,2003.
4. Phillip E.Allen, DouglasR.Holberg, ―CMOS Analog Circuit Design‖, Second Edition,Oxford University Press, 2002
5. A. Johns and Kenneth W. Martin, Tony Chan Carusone, David‖, Analog Integrated Circuit Design‖ Wiley 2011

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the concepts of single stage amplifier used in analog IC design

CO2

CO3 Familiarize the reference voltage biasing and current mirror circuits

CO4 Estimate the frequency response and noise analysis of single stage amplifiers

CO5 Analyze the performance of single and multistage opamps for IC design

Evaluate the stability and frequency compensation of Analog IC design

19VLE608	SIGNAL INTEGRITY FOR HIGH SPEED DEVICES	L	T	P	J	C
		3	0	0	0	3

UNIT-I FUNDAMENTALS **9**

The importance of signal integrity-new realm of bus design-Electromagnetic fundamentals for signal integrity-max well equations common vector operators-wave propagations-Electro statics- magneto statics-Power flow and the poynting vector-Reflections of electromagnetic waves.

UNIT-II CROSS TALK **9**

Introduction -mutual inductance and capacitance-coupled wave equation-coupled line analysis modal analysis-cross talk minimization signal propagation in unbounded conductive media-classic conductor model for transmission model.

UNIT-III DI-ELECTRIC MATERIALS **9**

Polarization of Dielectric-Classification of Di electric material-frequency dependent di electric material- Classification of Di electric material fiber-Weave effect-Environmental variation in dielectric behavior Transmission line parameters for loosy dielectric and realistic
conductors.

UNIT-IV DIFFERENTIAL SIGNALING **9**

Removal of common mode noise-Differential Cross talk-Virtual reference plane-propagation of model voltages common terminology-drawbacks of Differential signaling.

UNIT-V PHYSICAL TRANSMISSION LINE MODEL **9**

Introduction- non ideal return paths-Vias-IO design consideration-Push-pull transmitter- CMOS receivers-ESSD protection circuits-On chip Termination

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Advanced Signal Integrity for High-Speed Digital Designs By Stephen H. Hall, Howard L. Heck

2 Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS by JamesEdgar Buchanan

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the fundamentals of signal integrity for high speed devices

CO2 Analyze the crosstalk in inductive and capacitive modeled high speed devices

CO3 Estimate the behavior of dielectric materials and its characteristics

CO4 Infer the differential signal techniques used in high speed devices

CO5 Illustrate the concepts physical transmission model by push-pull transmitter and receivers

19VLE609	ASIC AND FPGA DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT-I INTRODUCTION TO ASICS, CMOS LOGIC, ASIC LIBRARY DESIGN **9**

Types of ASICs - Design flow – CMOS transistors- CMOS Design rules –Combinational logic Cell Sequential logic cell - Transistor as Resistors - Transistor parasitic capacitance – Logical effort - Library cell design – Library architecture.

UNIT-II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLSAND PROGRAMMABLE ASIC I/O CELLS **9**

Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Xilinx I/O blocks.

UNIT-III PROGRAMMABLE ASIC INTERCONNECT, ROGRAMMABLE ASICDESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY **9**

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Low level design language - PLA tools EDIF- CFI design representation.

UNIT-IV SILICON ON CHIP DESIGN **9**

Voice over IP SOC - Intellectual Property – SOC Design challenges- Methodology and design- FPGA to ASIC conversion – Design for integration-SOC verification -Set top box SOC

UNIT-V PHYSICAL AND LOW POWER DESIGN **9**

Over view of physical design flow- tips and guideline for physical design- modern physical design techniques- power dissipation-low power design techniques and methodologies-low power design tools- tips and guideline for low power design.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 M.J.S. Smith, Application Specific Integrated Circuits, Pearson Education, 2008.

2 FarzadNekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach,Prentice Hall PTR, 2003

3 Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2009.

4 Rajsuman, System-on-a-Chip Design and Test, Santa Clara, CA: Artech House Publishers,2000.

5 F.Nekoogar, Timing Verification of Application-Specific Integrated Circuits (ASICs), Prentice Hall PTR, 1999

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Classify the types of asics and the ASIC library design

CO2 Relate the PROM technologies in Xilinx and Altera FPGA market.

CO3 Understand the concepts of ASIC interconnects and software used in PLA design

CO4 Evaluate the SOC design challenges and design for integration in applications

CO5 Model a low power circuit with satisfied physical design

19VLE610	DIGITAL VLSI DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT-I DEEP SUBMICRON DIGITAL IC DESIGN, TRANSISTORS ANDDEVICESMOS AND BIPOLAR, FABRICATION, LAYOUT AND SIMULATION **9**

Review of Digital Logic Gate Design-digital IC design-computer Aided Design of digital circuits-The MOS Transistor-Bipolar Transistor and circuits-IC Fabrication technology Layout basics-modeling the MOS transistor for circuit simulation-SPICE MOS level1 device model-BSIM3 model-additional effects in MOS transistors-SOI technology.

UNIT-II MOS INVERTER CIRCUITS, STATIC MOS GATE CIRCUITS **9**

Voltage transfer characteristics-noise margin definitions-resistive load inverter design NMOS transistors as load devices-CMOS inverter-pseudo-NMOS inverters-sizing inverters- tristate inverters-CMOS gate circuits-complex CMOS gates-XOR and XNOR gates-multiplexer circuits – Flip-flops and latches – D flip flops and latches – power dissipation in CMOS gates-power and delay trade-offs.

UNIT-III HIGH SPEED CMOS LOGIC DESIGN, TRANSFER GATE ANDDYNAMIC LOGIC DESIGN **9**

Switching time analysis – detailed load capacitance calculation – improving delay calculation with input slope - gate sizing for optimal path delay – optimizing path with logical effort – basic concepts of transfer gate – CMOS transmission gate logic – dynamic D latches and D flip-flops – domino logic –voltage bootstrapping.

UNIT-IV SILICON ON CHIP DESIGN **9**

Introduction-MOS decoders – static RAM cell design-SRAM column I/O circuitry –memory architecture content addressable memories-FPGA-dynamic Read-Write memories-Read Only memories-EPROMs and E2PROMs-flash memory-FRAMs interconnect RC delays-buffer insertion for very long wires-interconnect coupling capacitance-interconnect inductance- antenna effects.

UNIT-V PHYSICAL AND LOW POWER DESIGN **9**

Power distribution design-clocking and timing issues, phase-locked loops/delay-locked loops – low power design through voltage scaling – estimation and optimization of switching activity – reduction of switched capacitance – adiabatic logic circuits – ESD protection – input circuits – output circuits and L(di/dt) noise– on-chip clock generation and distribution – latch-ups and its prevention – fault types and models –controllability and observability – adhoc testable design techniques – scan based techniques – Built-In-Self Test(BIST) techniques – current monitoring IDDQ test.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1. David A Hodges, Horace G Jackson, Resve A Saleh, "Analysis and design of Digital IntegratedCircuits – in deep submicron technology", Tata McGraw Hill, Edition-2005
2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits-analysis and design",Tata McGraw Hill, Third edition-2003
3. Uyemura, Chip design of Submicron VLSI: CMOS Layout and Simulation, ThomsonEngineering, 2005

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Relate various models and simulators to design digital ics

CO2 Understand the fundamental concepts of high speed CMOS and dynamic logic design.CO3: analyze the

CO3 switching time and optimization of dynamic logic design

CO4 Familiarize the RAM and ROM memory devices used for interconnect design.

CO5 Estimate the delay by pipelining,clock,timing issues and testability of faulty circuits.

Relate various models and simulators to design digital ics

19VLE611	CMOS MIXED SIGNAL CIRCUIT DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT-I VLSI AND ITS ALLIED FIELD **9**

Introduction to Active Filters (PLL) & Switched capacitor filters Active RC Filters for monolithic filer design: First & Second order filter realizations - universal active filter (KHN) - self tuned filter - programmable filters - Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample & hold circuits – Integrator- Biquad.

UNIT-II CONTINUOUS TIME FILTERS& DIGITAL FILTERS **9**

Introduction to Gm - C filters - bipolar transconductors - CMOS Transconductors using Triode transistors, active transistors – BiCMOS transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance - Digital Filters: Sampling – decimation – interpolation - implementation of FIR and IIR filters.

UNIT-III DIGITAL TO ANALOG & ANALOG TO DIGITAL CONVERTERS **9**

Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's. Sigma Delta Converters: Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's.

UNIT-IV ANALOG AND MIXED SIGNAL EXTENSIONS TO VHDL **9**

Introduction - Language design objectives - Theory of differential algebraic equations - the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples.

UNIT-V ANALOG EXTENSIONS TO VERILOG **9**

Introduction –data types –Expressions-Signals-Analog Behavior-Hierarchical structures-Mixed Signal Interaction. Introduction - Equation construction - solution - waveform Filter functions - simulator - Control Analysis - Multi -disciplinary model.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1. David a. Johns, ken martin, "analog integrated circuit design" john wiley & sons, 2002.
2. Rudy van de Plassche "Integrated Analog-to-Digital and Digital-to-Analog Converters", Kluwer 1999
3. Antoniou, "Digital Filters Analysis and Design" Tata mcgraw Hill, 1998.
4. Phillip Allen and Douglas Holmberg "CMOS Analog Circuit Design" Oxford University.Press, 2000
5. Benhardrazavi, "Data Converters", Kluwer Publishers, 1999

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the concepts of active and programmable filters in mixed signal circuits
CO2 Familiarize the digital and continuous time filters used in mixed signal circuits
CO3 Infer the need of ADC/DAC in mixed signal circuits to improve linearity
CO4 Relate the techniques used for analog and mixed signal extensions to VHDL
CO5 Relate the techniques used for analog and mixed signal extensions to verilog.

19VLE612	RF VLSI DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT-I PERFORMANCE PARAMETERS OF RF CIRCUITS 9

Gain Parameters, Non-linearity parameters, Noise figure, Phase Noise, Dynamic range, RF front end performance parameters, performance trade offs in an RF circuit.

UNIT-II FILTER DESIGN 9

Modern filter design, Frequency and impedance scaling, High Pass filter design, Band pass filter design, Band reject filter design, the effects of finite Q.

UNIT-III HIGH FREQUENCY AMPLIFIER DESIGN 9

Zeros as Bandwidth enhances, Shunt-series Amplifier, Bandwidth enhancement with frequency Doublers, Tuned amplifiers, Neutralization and unilateralization, cascaded Amplifiers, LNA Topologies.

UNIT-IV MIXERS AND OSCILLATORS 9

Mixer fundamentals, Non linear systems as Linear mixers, multiplier based mixers, Sub sampling mixers. Problems with purely linear oscillators, Tuned oscillator, Negative Resistance oscillators, frequency synthesis.

UNIT-V RF POWER AMPLIFIERS 9

General considerations, Class A, AB, B & C Power amplifier, Class D, E & F amplifiers, modulation of power amplifiers, RF Power amplifier design examples.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Aleksandar Tasic, Wouter.A.Serdijn, John.R.Long, "Adaptive Low Power Circuits for Wireless Communication (Analog Circuits and Signal Processing)",Springer, 1st Edition, 2006

2 Chris Bowick, "RF Circuit design", Newnes (An imprint of Elesvier Science), 1st Edition, 1997.

3 Thomas.H. Lee, "The design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2ndEdition, 2004. John Wiley and Sons, 2001

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Estimate various performance parameters of RF circuits

CO2 Design a filter with better quality factor in high frequency devices

CO3 Understand various types of high frequency amplifiers used in RF design

CO4 Familiarize the concepts of mixers and oscillators based on applications

CO5 Infer the types of Power amplifiers and its characteristics.

19VLE701	DESIGNING WITH CPLD & FPGA	L	T	P	J	C
		3	0	0	0	3

UNIT-I OVERVIEW OF VLSI DESIGN METHODOLOGY 9

VLSI design process - Architectural design - Logical design - Physical design - Layout styles - Full custom, Semicustom approaches.

UNIT-II COMBINATIONAL CIRCUITS 9

Shannon's expansion theorem - Design using Multiplexers, Decoders - Design of static hazard free and dynamic hazard free logic circuits

UNIT-III SEQUENTIAL CIRCUITS 9

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards- Unger's theorem.

UNIT-IV PROGRAMMABLE LOGIC DEVICES 9

Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Design of state machine using Algorithmic State Machines (ASM) chart as a design tool.

UNIT-V CPLDS AND FPGAS 9

Architectures of CPLDs and FPGAs.- Design of combinational and sequential circuits using CPLDs and FPGAs- Design examples

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1. Charles H Roth, " Digital system Design with VHDL", Thomson, 1998
2. James E Palmer and David E Perlman, "Introduction to Digital Systems ", Tata McGraw Hill, 1996.
3. Robert Dueck, "Digital design with CPLD applications and VHDL", Thomson, 2004
4. Bob Zeidman, "Designing with CPLDs and FPGAs", CMP, 2002.
5. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Addison-Wesley Professional, 1st Edition, 1997.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 understand the fundamental concepts of VLSI design process and methodology.
CO2 analyze and design hazard free combinational circuits with theorems.
CO3 analyze and design hazard free sequential circuits with theorems.
CO4 Infer the types and functions of Programmable Logic devices
CO5 Examine the architecture of CPLD and FPGA with examples.

19VLE702	EMBEDDED SYSTEM DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT-I EMBEDDED ARCHITECTURE 9

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded System Design, Embedded System Design Process - Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration.

UNIT-II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9

ARM Embedded Systems, ARM Processor Fundamentals –ARM organization and implementation –ARM CPU cores, ARM support for system development-ARM support for Operating Systems.

UNIT-III REAL-TIME OPERATING SYSTEM CONCEPTS 9

Embedded and Real-Time Systems-Introduction to Real-Time Operating Systems-Brief history of operating systems-Defining an RTOS-The Scheduler-Objects-Services-Key Characteristics of an RTOS-System using RTOS-RTOS concepts and definitions-RTOS building blocks for system development

UNIT-IV EMBEDDED SYSTEM DESIGN USING MSP430 9

Introduction- Architecture: CPU and Memory-Hardware considerations- Instruction set-Flash memory-Functions, Interrupts and Low power modes-Timers-Analog input and output.

UNIT-V EMBEDDED NETWORKS 9

Distributed Embedded Architecture - Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link ports, Ethernet, Myrinet, Internet. Design Example: Elevator Controller.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1. Wayne Wolf, Computers as Components: Principles of Embedded Computing System Design,Morgan Kaufman Publishers, 2001
2. Steve Furber, ‘’ ARM System –On –Chip architecture “Addison Wesley, 2000.
3. Andrew N. Sloss, “ARM System Developer’s Guide: Designing and Optimizing System Software , by Elsevier 2004.
4. Andrew N. Sloss, “ARM System Developer’s Guide: Designing and Optimizing System Software , by Elsevier 2004.
5. Chris Nagy “Embedded System Design using the TI MSP430 Series”,by Elsevier 2003

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Infer the characteristics of embedded systems with real time applications.
CO2 Understand the ARM processor fundamentals and its support operating systems.
CO3 Familiarize the RTOS definitions and its applications in system development.
CO4 Examine the functions and hardware controls of MSP430 in Embedded systems.
CO5 Classify the networks used in hardware and software embedded networks.

19VLE703	VLSI ARCHITECTURE FOR IMAGE AND VIDEO PROCESSING	L	T	P	J	C
		3	0	0	0	3

UNIT-I IMAGE PROCESSING ALGORITHMS 9

Introduction – Image Processing Tasks- Low level Image Processing Operations – Description of some intermediate level operations –Requirements for Image processorarchitecture.

UNIT-II IMAGE PROCESSING ARCHITECTURES AND PIPELINED LOWLEVEL IMAGE PROCESSING 9

Classification of Architectures – Uni and Multi processors – MIMD systems – SIMD systems – Pipelines – Devices for cellular logic processing – Design aspects of real time low level image processors –Design method for special architectures.

UNIT-III PIPELINED ARCHITECTURES & 2D AND 3D IMAGE PROCESSINGARCHITECTURES 9

Architecture of a cellular logic processing element – Second decomposition in data path and control – Real time pipeline for low level image processing – Design aspects of Image Processing architectures – Implementation of Low level 2D and 3D and Intermediate level algorithms.

UNIT-IV VIDEO PROCESSING ALGORITHMS 9

Motion Estimation Algorithms – Complexity Analysis Methodology –Complexity analysis of MPEG – 4 Visual – Analysis of Fast Motion Estimation Algorithms.

UNIT-V VLSI ARCHITECTURES FOR VIDEO PROCESSING 9

General design space evaluation – Design space motion estimation architectures – Motion estimation architectures for MPEG-4 – Design Tradeoffs – VLSI Implementation search engine I and Search engine II.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Peter M. Kuhn, ―Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4Motion Estimation ", Springer ISBN 978-1–4419-5088-8, First Edition, 2010

2 Pieter Jonker, ―Morphological Image Processing: Architecture and VLSI design‖, Springer. ISBN: 9020127667, First Edition, 1992

3 Rafael C. Gonzalez & Richard E. Woods, ―Digital Image Processing‖, Prentice Hall;Third edition, 2007

4 A.MuratTekalp, ―Digital Video Processing‖, Pearson Education, Noida, First Edition, 2010.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Analyze the algorithms and operations of VLSI image processors

CO2 Classify the types of image processing architectures and its design methodologies

CO3 Infer the functions of pipelined, 2D and 3D algorithms in image processors

CO4 Estimate the complexity of video processing by motion estimation algorithms

CO5 Understand the design tradeoff of videos using VLSI architecture

19VLE704	RECONFIGURABLE COMPUTING	L	T	P	J	C
		3	0	0	0	3

UNIT-I DEVICE ARCHITECTURE **9**

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs– Device Architecture - Case Studies.

UNIT-II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS **9**

Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.

UNIT-III PROGRAMMING RECONFIGURABLE SYSTEMS **9**

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing –Operating System Support for Reconfigurable Computing

UNIT-IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS **9**

The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bitstream Generation – Case Studies with Appropriate Tools.

UNIT-V APPLICATION DEVELOPMENT WITH FPGA **9**

Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.

2 Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing – The Theory and Practiceof FPGA-Based Computation", Elsevier / Morgan Kaufmann, 2008.

3 ChristopheBobda, "Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications", Springer, 2010.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Compare the architecture of general purpose and reconfigurable CPLD and fpgas

CO2 Understand the reconfigurable computing systems with real time applications

CO3 Model and compute the FPGA applications in reconfigurable architectures

CO4 Develop mapping designs by routing and floor plan for reconfigurable architectures.

CO5 Apply the reconfigurable computations with FPGA in sopc design

19VLE705	IP BASED VLSI DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT-I VLSI AND ITS FABRICATION 9

Introduction, IC manufacturing, CMOS technology, IC design techniques, IP based design, Fabrication process-Transistors, Wires and Via, Fabrication Theory reliability, Layout Designand tools.

UNIT-II COMBINATIONAL LOGIC NETWORKS 9

Logic Gates: Combinational Logic Functions, Static Complementary Gates, Switch Logic, Alternate Gate circuits, Low power gates, Delay, Yield, Gates as IP, Combinational Logic Networks-Standard Cell based Layout, Combinational network delay, Logic and,Interconnect design, Power optimization, Switch logic network, logic testing.

UNIT-III SUBSYSTEM DESIGN 9

Sequential Machine-Latch and Flip flop, System design and Clocking, Performance analysis, power optimization, Design validation and testing; Subsystem Design- Combinational Shifter, Arithmetic Circuits, High Density memory, Image Sensors,FPGA,PLA, Buses and NoC, Data paths, Subsystems as IP.

UNIT-IV FLOOR PLANNING AND ARCHITECTURE DESIGN 9

Floor planning-Floor planning methods, Global Interconnect, Floor plan design, Off-chip Connections Architecture Design- HDL, Register-Transfer Design, Pipelining, High Level Synthesis, Architecture for Low power, GALS systems, Architecture Testing, IP,Components, Design Methodologies, Multiprocessor System-on-chip Design.

UNIT-V DESIGN SECURITY 9

IP in reuse based design, Constrained based IP protection, Protection of data and Privacy constrained based watermarking for VLSI IP based protection

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Wayne wolf, "Modern VLSI Design:IP-based Design", Pearson Education,2009.

2 Qu gang, "Intellectual Property Protection in VLSI Designs: Theory and Practice", kluwer academic publishers,2003.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 relate the basic concepts of IC fabrication techniques with layout design and tools

CO2 Analyze the delay and power optimization in combinational logic networks.

CO3 estimate the clocking issues and system performance of sequential logic and its subsystems

CO4 Infer the methods of floor plan and low power design methodologies in

CO5 MultiprocessorSoC classify the types of IP based protection techniques for VLSI design security

19VLE706	SECURITY SOLUTIONS IN VLSI	L	T	P	J	C
		3	0	0	0	3

UNIT-I BASIC CONCEPTS **9**

Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism inOS, Targets: Hardware, Software, Data communication procedures. Threats to Security: Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security.

UNIT-II ENCRYPTION TECHNIQUES **9**

Conventional techniques, Modern techniques, DES, DES chaining+, Triple DES, RSA algorithm, Key management. Message Authentication and Hash Algorithm: Authentication requirements and functions secure Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service.

UNIT-III FIREWALLS AND CYBER LAWS **9**

Firewalls, Design Principles, Trusted systems, IT act and cyber laws, Virtual private network.

UNIT-IV FUTURE THREATS TO NETWORK **9**

Recent attacks on networks, VLSI Based Case study

UNIT-V CRYPTO CHIP DESIGN **9**

VLSI Implementation of AES algorithm. Implementation of DES, IDEA AES algorithm, Development of digital signature chip using RSA algorithm.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 William Stalling "Cryptography and Network Security" Pearson Education, 2005

2 Charels P. Pfleeger "Security in Computing" Prentice Hall, 2006

3 Jeff Crume "Inside Internet Security" Addison Wesley, 2000

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the basic concepts of threats, monitoring control and security systems.

CO2 familiarize the encryption techniques and algorithm used for message authentication

CO3 familiarize the encryption techniques and algorithm used for message authentication

CO4 relate the recent attacks and threats in VLSI networks with real time examples

CO5 develop the digital signature chip for security using various security algorithms

19VLE707	POWER EFFICIENT VLSI DESIGN	L	T	P	J	C
		3	0	0	0	3

UNIT I POWER DISSIPATION IN CMOS **9**

Sources of power Dissipation–Physics of power dissipation in MOSFET devices, Power dissipation in CMOS, Low power VLSI design limits.

UNIT II ARCHITECTURES FOR NOCS **9**

Shared medium networks, direct networks, indirect networks, Hybrid networks, Standard architectures and formal properties, Network architectures for on-chip realization, Ad hoc network architectures.

UNIT III PHYSICAL NETWORK AND DATA-LINK LAYER **9**

Wiring issues, Physical routing, Signaling, Driver/receiver design, Noise immunity, Shielding, Medium access control, Data encoding, Error correcting codes: theory and practice, Arbitration issues.

UNIT IV NETWORK AND TRANSPORT LAYERS **9**

Packets, Flits, Switching techniques, No topologies, Routing algorithms and routers, QoS guarantees, Congestion and Flow control.

UNIT V SOFTWARE AND TOOLS FOR NOCS **9**

Programming paradigms- shared medium vs. message passing, Middleware issues- layering and software encapsulation, Application layer issue and network-aware compilation, Analysis and Synthesis of NoCs,Present tools (Bones, Xpipes) and future outlook..

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Giovanni De Micheli and Luca Benini ‘Networks on Chips: Technology and Tools’, Academic Press,2006

2 Axel Jantsch, Hannu Tenhunen ‘Networks on Chips’, Springer, 2003.

3 Davide Bertozzi, Shashi Kumar, Maurizio Palesi ‘Networks on Chips’, Hindawi Publishing Corporation,2007.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Infer the basic concepts of power dissipation in Low power VLSI circuits.

CO2 Identify the types of network architectures for on ship system design

CO3 Analyze the issues and practices in physical and data link layer.

CO4 Predict the algorithms and techniques to counter network traffic congestion

CO5 Analyze the application layer and networking issues using tools and programming paradigms

19VLE708	NANOTECHNOLOGY	L	T	P	J	C
		3	0	0	0	3

UNIT-I BASICS OF NANOELECTRONICS 9

Basics of nano electronics – capabilities of nano electronics – physical fundamentals of nano electronics – basics of information theory – the tools for micro and nano fabrication – basics of lithographic techniques for nano electronics

UNIT-II QUANTUM ELECTRON DEVICES 9

Quantum electron devices – from classical to quantum physics: upcoming electronic devices – electrons in mesoscopic structure – short channel MOS transistor – split gate transistor – Electron wave transistor – Electron spin transistor – quantum cellular automate – quantum dot array – Principles of Single Electron Transistor (SET) – SET circuit design – comparison between FET and SET circuit design.

UNIT-III NANOELECTRONICS WITH TUNNELING DEVICES ANDSUPERCONDUCTING DEVICES 9

Nanoelectronics with tunneling devices and superconducting devices – tunneling element technology - RTD: circuit design – Defect tolerant circuits - Molecualr electronics – elementary circuits – flux quantum devices – application of Superconducting devices – Nanotubes based sensors, fluid flow, gas, temperature, Strain – oxide nanowire, gas sensing (ZnO, TiO, SnO, WO), LPG sensor (SnO powder)- Nano 2 2 3 2 designs and Nanocontacts - metallic nanostructures.

UNIT-IV SURVEY ON NANOTECHNOLOGY 9

A survey about the limits – Replacement Technologies – Energy and Heat dissipation – Parameter spread as Limiting Effect – Limits due to thermal particle motion – Reliability as limiting factor – Physical limits – Final objectives of integrated chip and systems.

UNIT-V MEMORY DEVICES AND SENSORS 9

Memory devices and sensors – Nano ferroelectrics – Ferroelectric random access memory – Fe- RAM circuit design – ferroelectric thin film properties and integration – calorimetric sensors – electrochemical cells – surface and bulk acoustic devices – gas sensitive FETs – resistive semiconductor gas sensors –electronic noses – identification of hazardous solvents and gases – semiconductor sensor array.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 K.Goser, P.Glosekotter & J.Dienstuhl, "Nanoelectronic and Nanosystems – From Transistorsto Molecular Quantum Devices" Springer

2 Rainer Waser, "Nanoelectronics and Information Technology: Advanced Electronic MaterialsNovel and Devices" Wiley VCH

3 Mick Wilson, KamaliKannangara, Geoff smith, "Nanotechnology: Basic Science and Emerging Technologies", Overseas press

4 W.R. Fahrner, "Nanotechnology and Nanoelectronics: Materials, Devices, MeasurementTechniques", Springer, 2010

5 Branda Paz, "A Handbook on Nanoelectronics", Vedams books, 2008

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the fundamental concepts of nano electronics and its fabrication techniques

CO2 Infer the types of quantum electronic devices and its principles of operation.

CO3 Classify the nano electronics with tunneling devices and superconducting devices with itsapplications

CO4 Examine the physical and reliability limitations of nano electronic devices

CO5 Familiarize the properties and characteristics of nano memory device and sensors

19VLE709	NETWORK ON CHIP	L	T	P	J	C
		3	0	0	0	3

UNIT I INTRODUCTION AND MOTIVATION **9**

SoC objectives and NoC needs, State of the art Taxonomy, Technology trends, Characteristics of NoCs, Component design for NoCs, Properties of network architectures.

UNIT II LOW POWER ADDERS AND MULTIPLIERS **9**

Standard adder cells, CMOS adder architectures, BiCMOS adder, overview and types of Multipliers-Braun Multiplier, Baugh – WooleyMultiplier, Wallace Tree Multiplier, Booth Multiplier

UNIT III SYNTHESIS FOR LOW POWER **9**

Behavioral level transforms-Algorithm using First –Order, second, Mth Order Differences- Parallel Implementation Pipelined Implementation- Logic level optimization– Technology dependent and Independent– -Circuit level- Static, Dynamic, PTL,DCVSL,PPL

UNIT IV LOW POWER STATIC RAM ARCHITECTURES **9**

Organization of a static RAM, MOS static RAM memory cell, Banked organization of SRAMs, Reducing voltage swings on bit lines, Reducing power in the write diver circuits, Reducing power in sense amplifier circuits.

UNIT V LOW ENERGY COMPUTING USING ENERGY RECOVERYTECHNIQUES **9**

Energy dissipation in transistor channel using an RC model, Energy recovery circuit design, Designs with partially reversible logic, Supply clock generation.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 K.Roy and S.C. Prasad, Low Power CMOS VLSI Circuit Design, Wiley, 2000

2 K.S. Yeo and K.Roy, Low-Voltage, Low-Power VLSI Subsystems, Tata McGraw-Hill, 2004.

3 DimitriosSoudris, ChirstianPignet and Costas Goutis, Designing CMOS Circuits for Low Power, Kluwer, 2009

4 James B. Kuo and Shin – Chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits, John Wiley and Sons, 2001

5 J.B Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley, 1999.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the fundamental concepts of Network on Chip design

CO2 Infer the techniques used to design adders and multipliers architectures.

CO3 Analyze and synthesis the low power VLSI circuits of various levels of abstraction

CO4 Examine the banked organization of low power static RAM architectures

CO5 Model a low power circuits with energy recovery techniques

19VLE710	SCRIPTING LANGUAGES FOR VLSI	L	T	P	J	C
		3	0	0	0	3

UNIT I INTRODUCTION TO SCRIPTING AND PERL 9

Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT II ADVANCED PERL 9

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems,

Security issues.

UNIT III TCL 9

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT IV ADVANCED TCL 9

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running un trusted code, The C interface.

UNIT V TK AND JAVA SCRIPT 9

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Brent Welch,"Practical Programming in Tcl and Tk",Fourth Edition, 2003.
2 David Barron, "The World of Scripting Languages", Wiley Publications, 2000.
3 Guido van Rossum, and Fred L. Drake ", Python Tutorial, Jr., editor, Release 2.6.4
4 Randal L. Schwartz, "Learning PERL", Sixth Edition, O'ˇReilly

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the characteristics of PERL and its functions parameters
CO2 Infer the subroutines and interfacing modules of PERL with OS
CO3 Familiarize the concepts of TCL and its procedures with examples
CO4 Evaluate the advanced TCL with security issues and event driven circuits
CO5 Relate various scripting language with Object oriented programming

19VLO701	MEMS AND ITS APPLICATIONS	L	T	P	J	C
		3	0	0	0	3

UNIT-I MEMS AND MICROSYSTEMS **9**

MEMS and Microsystems products, evaluation of micro fabrication, micro-systems and microelectronics, applications of Microsystems, working principles of Microsystems, micro- sensors, micro-actuators, MEMS and micro-actuators, micro-accelerometers. Scaling Laws In Miniaturization: Introduction, scaling in geometry, scaling in rigid body dynamics, the trimmer force scaling vector, scaling in electrostatic forces.

UNIT-II MATERIALS FOR MEMS AND MICROSYSTEMS **9**

Substrates and wafers, silicon as a substrate material, ideal substrates for MEMS, single crystal silicon and wafers crystal structure, mechanical properties of Si, silicon compounds, SiO2, SiC, Si3N4. And polycrystalline Silicon, silicon piezo resistors, gallium arsenide, quartz, piezoelectric crystals, polymers for MEMS, conductive polymers.

UNIT-III ENGINEERING MECHANICS FOR MICROSYSTEMS DESIGN **9**

Introduction, static bending of thin plates, circular plates with edge fixed rectangular plate with all edges fixed and square plates with all edges fixed. Mechanical vibration, resonant vibration, micro accelerometers, design theory d damping coefficients. Thermo mechanics, thermal stresses. Fracture mechanics, stress intensity factors, fracture toughness and interfacial fracture machine.

UNIT-IV BASICS OF FLUID MECHANICS IN MACRO AND MESO SCALES **9**

Viscosity of fluids, flow patterns Reynolds number. Basic equation in continuum fluid dynamics, laminar fluid flow in circular conduits, computational fluid dynamics, and incompressible fluid flow in micro conducts surface tension, capillary effect and micro pumping. Fluid flow in sub micrometer and nanoscale, rare field gas, kundsen and Mach number and modeling of micro gas flow, heat conduction in multilayered thin films.

UNIT-V MICROSYSTEM FABRICATION PROCESS **9**

Photolithography, photo resist and applications, light sources. Ion implantation, diffusion process, oxidation, thermal oxidation, silicon diode, thermal oxidation rates, Oxide thickness by colour. Chemical vapour deposition, principle, reactants in CVD, enhanced CVD physical vapour defusing, sputtering, deposition by epitaxial etching, chemical and plasma etching.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Tai-Ran Hus, MEMS and Microsystems Design and Manufacture, Tata McGraw-Hill, 2001.

2 John A Pelesko, Modeling MEMs and NEMS, CRC Press, 2002.

3 Chang Liu, Foundation of MEMS, Pearson Edition, 2005

4 Stephen Beeby, Graham Ensell, MEMS, Mechanical Sensors, Artech House Publishers, 2004.

5 Wanjun Wang, Steven A. Soper, Bio-MEMS Technologies and Applications, CRC Press,2007.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the fundamental concepts and working principles of MEMS and Microsystems

CO2 Infer the types of material used to design MEMS and microsystem devices

CO3 Analyze the physical and mechanical characteristics of MEMS devices

CO4 Evaluate the fluid mechanics of MEMS devices in macro and meso scales

CO5 Familiarize the techniques and process used to fabricate MEMS devices

19VLO702	BLUETOOTH TECHNOLOGY	L	T	P	J	C
		3	0	0	0	3

UNIT-I THE BLUETOOTH MODULE **9**

Introduction-overview - the Bluetooth module-antennas-baseband-introduction-Bluetooth device address – masters, slaves, and Pico nets-system timing-physical links-Bluetooth packet structure-logical channels frequency hopping.

UNIT-II THE LINK CONTROLLER **9**

The link controller-link control protocol-link controller operation-Pico net, scatter net operation master/slave role switching-base band/link controller architectural overview -link manager-the host controller interface.

UNIT-III THE BLUE TOOTH HOST **9**

The blue tooth host-logical link control and adaptation protocol –RFCOMM- the service discovery protocol –the wireless access protocol-OBEX and IrDA-telephony control protocol.

UNIT-IV CROSS LAYER FUNCTIONS **9**

Cross layer functions-Encryption and security-low power operations-controlling low power modes-hold mode sniff mode-park mode-quality of service-managing Bluetooth devices.

UNIT-V TEST AND QUALIFICATION **9**

Test and qualification- test mode-qualification and type approval-implementation – related standards and technologies.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Jennifer Bray, Brain Senese, Gordon McNutt, Bill Munday, " Bluetooth Application Developer's Guide", Syngress Media, 2001.

2 C S R Prabhu, P A Reddi, " Bluetooth Technology and its applications with JAVA andJ2ME", PHI ,2006

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Infer the fundamental concepts of Bluetooth technology in physical layer
CO2 Identify the operation of switching and interface link of Bluetooth technology
CO3 Understand the types of protocol used to access in wireless medium
CO4 Analyze the encryption and security solution in cross layer function
CO5 Describe the testing standards and technologies used in Bluetooth devices

19VLO703	MULTICORE PROCESSOR AND SYSTEMS	L	T	P	J	C
		3	0	0	0	3

UNIT-I MULTIPROCESSORS AND SCALABILITY ISSUES 9

Scalable design principles – Principles of processor design – Instruction Level Parallelism, Thread level parallelism - Parallel computer models –Symmetric and distributed shared memory architectures – Performance Issues – Multi-core Architectures - Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi- core architecture – SUN CMP architecture.

UNIT-II MULTICORE SYSTEMS ON-CHIP 9

MCSoCs Design Problems – SoC typical architecture- Multicore architecture Platform – Application specific MCSoC design method, Queue Core architecture: synthesis and evaluation,
Network-on-Chip –Router Architecture, Topology, Routing

UNIT-III LOW POWER AND RECONFIGURABLE CORES 9

Low Power Embedded QC2 Core - Architecture, Synthesis, Design Approach, Reconfigurable Multicore – Performance, Power Aware technological level optimizations - Power Aware system design optimizations - Hardware Adaptation, Software Adaptation, Future Directions

UNIT-IV PARALLEL PROGRAMMING 9

Fundamental concepts – Designing for threads – Scheduling -Threading and parallel programming constructs – Synchronization –Critical sections – Deadlock. Threading APIs

UNIT-V MULTITHREADED APPLICATION DEVELOPMENT 9

Multithreaded Applications – Algorithms – Dynamic Multithreading -Analysis of Multithreaded Algorithms, Parallel Loops, Race Condition -Performance measures - Program development and performance tuning

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 ShameemAkhter and Jason Roberts, Multi-core Programming, Intel Press, First Edition, 2006
2 Ben AbadallahAbderazek, Multicore Systems On-Chip : PracticalSoftware Hardware Design, Atlantis Press, Second Edition, 2010
3 Michael J Quinn, Parallel programming in C with MPI and Open MP, Tata McGraw Hill, FirstEdition, 2003.
4 John L. Hennessey and David A. Patterson,Computerarchitecture,A quantitative approach, Morgan Kaufmann Elsevier Publishers, Fourth Edition, 2007
5 David E. Culler and Jaswinder Pal Singh,Parallel computing architecture: A hardware software approach, Morgan Kaufmann/Elsevier Publishers, First Edition, 1999.

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Identify the types of multiprocessors based on applications and its performance issues
CO2 Understand the principles and performance of Multicore soc architecture.
CO3 Infer the low power multi core processors and its optimization techniques
CO4 Familiarize the fundamental concepts of parallel processing
CO5 Apply the algorithms in multithreaded applications to improve the performance of multicore Processors.

19VLO704	VLSI DESIGN TECHNIQUES	L	T	P	J	C
		3	0	0	0	3

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. Basic CMOS technology.

UNIT II INVERTERS CIRCUIT ANALYSIS 9

NMOS Inverters, Stick diagram, Inverter ratio, DC characteristics, Transient characteristics , Switching times, Super buffers, Driving large capacitance loads.

UNIT III CMOS LOGIC GATES 9

CMOS Inverters, CMOS logic structures, Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT IV CIRCUIT CHARACTERISATION AND PERFORMANCEESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation, Charge sharing.

UNIT V VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVELPHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits– Ripple carry adders, Carry look ahead adders, Multipliers, Physical design – Delay modeling, floor planning.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc.,2002.

2 Pucknell, “Basic VLSI Design”, Prentice Hall of India Publication, 2002.

3 Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, PearsonEducation ASIA, 2nd edition, 2002

4 Stephen Brown,zvonkovranesic,”Fundamentals of Digital Logic Design With VHDL”,Second Edition 2007

5 Kamaran,Eshraghian,Douglas.A.Pucknell,sholeheshkaghien,”Essentials of VLSI Circuits And Systems”,PHI Publications,2005

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the basic concepts of MOS transistor theory and its process technology

CO2 Analyze the CMOS inverter transient and switching characteristics

CO3 Infer the types of CMOS digital logic circuits to design a static and dynamic logic design

CO4 Estimate the power dissipation and low power performance of VLSI circuits

CO5 Model a system component of VLSI circuits in physical layer of abstraction

19VLO705	INTERNET OF THINGS	L	T	P	J	C
		3	0	0	0	3

UNIT I INTRODUCTION OF IoT **9**

Definition & Characteristics of IoT - Challenges and Issues - Physical Design of IoT, Logical Design of IoT - IoT Functional Blocks, Security.

UNIT II PROTOCOLS OF IoT **9**

Control Units – Communication modules – Bluetooth – Zigbee – Wifi – GPS- IOT Protocols (IPv6,6LoWPAN, RPL, CoAP etc.), MQTT, Wired Communication, Power Sources.

UNIT III PILLARS OF IoT **9**

Four pillars of IOT paradigm, - RFID, Wireless Sensor Networks, SCADA (Supervisory Control and Data Acquisition), M2M - IOT Enabling Technologies - BigData Analytics, Cloud Computing, Embedded Systems.

UNIT IV WEB OF THINGS **9**

Clustering, Clustering for Scalability, Clustering Protocols for IOT. The Future Web of Things –Set up cloud environment –Cloud access from sensors– Data Analytics for IOT- Case studies- Open Source ‘e-Health sensor platform’ – ‘Be Close Elderly monitoring’ – Other recent projects.

UNIT V APPLICATIONS OF IoT **9**

Working principles of sensors – IOT deployment for Raspberry Pi /Arduino/Equivalent platform – Reading from Sensors, Communication: Connecting microcontroller with mobile devices – communication through Bluetooth, wifi and USB - ContikiOSCooja Simulator.

L : 45 T: 0 P: 0 J: 0 Total: 45 PERIODS

REFERENCES

1 Dieter Uckelmann et.al, “Architecting the Internet of Things”, Springer, 2011

2 ArshdeepBahga and Vijay Madisetti, “Internet of Things – A Hand-on Approach”,Universities press, 2015.

3 Charalampos Doukas , "Building Internet of Things with the Arduino", Create space, April2002

4 Dr. OvidiuVermesan and Dr. Peter Friess, “Internet of Things: From research and innovationto market deployment”, River Publishers 2014

5 Contiki : The open source for IOT, www.contiki-os.org

COURSE OUTCOMES

At the end of the course student should be able to:

CO1 Understand the fundamental concepts of communication models and protocols in IOT

CO2 Relate the protocols used in wired and wireless mode of communication in IOT

CO3 Analyze the working principles of four pillars of iot with real time applications

CO4 Familiarize the concepts of Web of things and clustering protocols for communication

CO5 Infer the principles of sensors and communication protocols used in IOT devices