



# **SNS COLLEGE OF TECHNOLOGY**

**(An Autonomous Institution)**



**Approved by AICTE, Recognized by UGC & Affiliated to Anna University  
Accredited by NBA-AICTE, NAAC-UGC with 'A+' Grade**

**Saravanampatti, Coimbatore -641035**

## **CURRICULA AND SYLLABI REGULATION 2016 CHOICE BASED CREDIT SYSTEM**

### **DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

#### **M.E. – VLSI DESIGN**

**SNS COLLEGE OF TECHNOLOGY, COIMBATORE – 641035****(AN AUTONOMOUS INSTITUTION)****REGULATION – 2016****CHOICE BASED CREDIT SYSTEM****SUGGESTED CURRICULUM AND SYLLABI I – IV SEMESTERS****M. E. VLSI DESIGN****SEMESTER I**

S.NO.	COURSE CODE	COURSE TITLE	CAT	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
<b>THEORY</b>									
1.	16MA605	Applied Mathematics for Electronics Engineers	FC	4	3	1	0	4	-
2.	16VL601	Advanced Digital System Design	PC	4	3	1	0	4	-
3.	16VL602	Computer Aided Design for VLSI Circuits	PC	4	3	1	0	4	-
4.	16VL603	Design of Semiconductor Memories	PC	3	3	0	0	3	-
5.	16VL604	DSP Integrated Circuits	PC	3	3	0	0	3	-
6.		Elective-I	PE	3	3	0	0	3	-
<b>PRACTICAL</b>									
7.	16VL605	VLSI design- I Laboratory	PC	2	0	0	2	1	-
8.	16VL606	Industrial Training I	EEC	2	0	0	2	1	-
<b>TOTAL</b>				<b>25</b>	<b>18</b>	<b>3</b>	<b>4</b>	<b>23</b>	

**SEMESTER II**

S.NO.	COURSE CODE	COURSE TITLE	CAT	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
<b>THEORY</b>									
1.	16VL 607	Analog VLSI Design	PC	4	3	1	0	4	-

2.	16VL 608	Testing of VLSI Circuits	PC	4	3	1	0	4	-
3.	16VL609	Device Modeling	PC	3	3	0	0	3	-
4.		Elective-II	PE	3	3	0	0	3	-
5.		Elective-III	PE	3	3	0	0	3	-
<b>PRACTICAL</b>									
7.	16VL610	VLSI design- II Laboratory	PC	2	0	0	2	1	-
8.	16VL611	Industrial Training II	EEC	2	0	0	2	1	-
<b>TOTAL</b>				<b>21</b>	<b>15</b>	<b>2</b>	<b>4</b>	<b>19</b>	

### SEMESTER III

S.NO.	COURSE CODE	COURSE TITLE	CAT	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
<b>THEORY</b>									
1.		Elective-IV	PE	3	3	0	0	3	-
2.		Elective-V	PE	3	3	0	0	3	-
3.		Open Elective	OE	3	3	0	0	3	-
<b>PRACTICAL</b>									
4.	16VL701	Technical Seminar & Research Methodology	EEC	2	0	0	2	1	-
5.	16VL702	Project Phase-I	EEC	12	0	0	12	6	-
<b>TOTAL</b>				<b>23</b>	<b>9</b>	<b>0</b>	<b>14</b>	<b>16</b>	

### SEMESTER IV

S.NO.	COURSE CODE	COURSE TITLE	CAT	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
<b>THEORY</b>									
1.	16VL703	Project Phase-II	EEC	24	0	0	24	12	-
<b>TOTAL</b>				<b>24</b>	<b>0</b>	<b>0</b>	<b>24</b>	<b>12</b>	

**TOTAL CREDITS OF THE PROGRAMME : 70**

### FOUNDATION COURSE (FC)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
1.	16MA605	Applied Mathematics for Electronics Engineers	4	3	1	0	4	-

TOTAL				3	1	0	4	
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### PROFESSIONAL CORE (PC)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
1.	16VL601	Advanced Digital System Design	4	3	1	0	4	-
2.	16VL602	Computer Aided Design for VLSI Circuits	4	3	1	0	4	-
3	16VL603	Design of Semiconductor Memories	3	3	0	0	3	-
4	16VL604	DSP Integrated Circuits	3	3	0	0	3	-
5	16VL607	Analog VLSI Design	4	3	1	0	4	-
6	16VL608	Testing of VLSI Circuits	4	3	1	0	4	-
7	16VL609	Device modeling	3	3	0	0	3	-
<b>PRACTICAL</b>								
8	16VL605	VLSI design- I Laboratory	2	0	0	2	1	
9	16VL610	VLSI design- II Laboratory	2	0	0	2	1	
TOTAL				12	4	4	27	

### PROFESSIONAL ELECTIVES (PE)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
1.	16VL612	Reconfigurable computing	3	3	0	0	3	-
2.	16VL613	VLSI Architecture for Image and Video Processing	3	3	0	0	3	-
3.	16VL614	Hardware Description Language	3	3	0	0	3	-
4.	16VL615	Digital VLSI Design	3	3	0	0	3	-
5.	16VL616	Embedded System Design	3	3	0	0	3	-
6.	16VL617	Designing with CPLD and FPGA	3	3	0	0	3	-

7.	16VL618	IP based VLSI Design	3	3	0	0	3	-
8.	16VL619	System on chip	3	3	0	0	3	-
9.	16VL620	DSP Processors Architecture and Programming	3	3	0	0	3	-
10.	16VL621	RF VLSI DESIGN	3	3	0	0	3	-
11.	16VL622	VLSI For Wireless Communication	3	3	0	0	3	-
12.	16VL623	Nanotechnology	3	3	0	0	3	-
13.	16VL624	Security solutions in VLSI	3	3	0	0	3	-
14.	16VL625	ASIC and FPGA Design	3	3	0	0	3	-
15.	16VL626	Signal integrity for high speed devices	3	3	0	0	3	-
16.	16VL710	VLSI technology	3	3	0	0	3	-
17.	16VL711	Physical Design Of VLSI circuits	3	3	0	0	3	-
18.	16VL712	Analysis and Design of Analog Integrated Circuits	3	3	0	0	3	-
19.	16VL713	CMOS Mixed Signal Circuit Design	3	3	0	0	3	-
20.	16VL714	Power Efficient VLSI Design	3	3	0	0	3	-
		TOTAL	15	15	0	0	15	

#### EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
1	16VL606	Industrial Training I	2	0	0	2	1	-
2	16VL611	Industrial Training II	2	0	0	2	1	-
3	16VL701	Technical Seminar & Research Methodology	2	0	0	2	1	-
4	16VL702	Project Phase-I	12	0	0	12	6	-
5	16VL703	Project Phase-II	24	0	0	24	12	-
TOTAL				0	0	42	21	

### OPEN ELECTIVE OFFERED TO OTHER PG PROGRAMMES

S.NO.	COURSE CODE	COURSE TITLE	CONTACT PERIODS	L	T	P	C	PRE-REQUISITES
1.	16VL001	MEMS and its Applications	3	3	0	0	3	-
2.	16VL002	Bluetooth Technology	3	3	0	0	3	-
3.	16VL003	Multi core processor and systems	3	3	0	0	3	-
4.	16VL004	VLSI Design Techniques	3	3	0	0	3	-
5.	16VL005	Internet of Things	3	3	0	0	3	-
		TOTAL	3	3	0	0	3	

S.No.	SUBJECT AREA	Credits Per Semester				Total Credits
		I	II	III	IV	
1	FC	4				4
2	PC	15	12			27
3	PE	3	6	6		15
4	OE			3		3
5	EEC	1	1	7	12	21
	<b>TOTAL</b>	<b>23</b>	<b>19</b>	<b>16</b>	<b>12</b>	<b>70</b>

<b>16MA605</b>	<b>APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS</b> (M.E VLSI)	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>1</b>	<b>0</b>	<b>4</b>
<b>UNIT I</b>	<b>FUZZY LOGIC</b>				<b>9+3</b>
Classical logic – Multi valued logics – Fuzzy propositions – Fuzzy quantifiers.					
<b>UNIT II</b>	<b>MATRIX THEORY</b>				<b>9+3</b>
Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition – Toeplitz matrices and some applications					
<b>UNIT III</b>	<b>ONE DIMENSIONAL RANDOM VARIABLES</b>				<b>9+3</b>
Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.					
<b>UNIT IV</b>	<b>DYNAMIC PROGRAMMING</b>				<b>9+3</b>
Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.					
<b>UNIT V</b>	<b>QUEUEING MODELS</b>				<b>9+3</b>
Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.					
		<b>L:45</b>	<b>T:15</b>	<b>P: 0</b>	<b>Total: 60 PERIODS</b>

#### REFERENCES

- 1 George.J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 2011
- 2 Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2007
- 3 Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 8<sup>th</sup> Edition, Prentice – Hall of India, Private Ltd., New Delhi
- 4 Taha, H.A. Operations Research: An Introduction, Ninth Edition, Pearson Education Edition, Asia, New Delhi, 2011
- 5 Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 3<sup>rd</sup> edition, John Wiley and Sons, New York

#### COURSE OUTCOMES

At the end of the course student should be able to:

- CO1** Convert an Engineering statement problem into a mathematical probabilistic Statement.
- CO2** Know how to compute certain matrix decompositions and some of their applications.
- CO3** Calculate standard statistics from mass, distribution and density functions.
- CO4** Recognize, interpret and apply a variety of random processes that occur in engineering.
- CO5** Acquire adequate knowledge in the field of Fuzzy logic.

<b>16VL601</b>	<b>ADVANCED DIGITAL SYSTEM DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>1</b>	<b>0</b>	<b>4</b>
<b>UNIT I</b>	<b>SEQUENTIAL CIRCUIT DESIGN</b>				<b>9+3</b>
Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuit- design of iterative circuits-ASM chart and realization using ASM.					
<b>UNIT II</b>	<b>ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN</b>				<b>9+3</b>
Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.					
<b>UNIT III</b>	<b>FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS</b>				<b>9+3</b>
Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.					
<b>UNIT IV</b>	<b>SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES</b>				<b>9+3</b>
Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.					
<b>UNIT V</b>	<b>SYSTEM DESIGN USING VHDL</b>				<b>9+3</b>
VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.					
		<b>L : 45</b>	<b>T: 0</b>	<b>P: 0</b>	<b>J: 0 Total: 45 PERIODS</b>

#### REFERENCES

- 1 Charles H.RothJr “Fundamentals of Logic Design” Thomson Learning 2005.
- 2 Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001.
- 3 ParagK.Lala “Fault Tolerant and Fault Testable Hardware Design” BS Publications,2002
- 4 Parag K.Lala “Digital system Design using PLD” B S Publications,2003.
- 5 Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004.

#### COURSE OUTCOMES

At the end of the course student should be able to:

- CO1** understand the concepts of sequential circuits and its modeling techniques
- CO2** analyze the asynchronous circuit design and types of hazards in circuit design
- CO3** familiarize the algorithmic methods used for fault diagnosing and testing in digital circuits
- CO4** Infer the families of PLDs and its types with applications.
- CO5** Apply the system design of digital circuits using VHDL programming.



<b>16VL602</b>	<b>COMPUTER AIDED DESIGN FOR VLSI CIRCUITS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>1</b>	<b>0</b>	<b>4</b>
<b>UNIT I</b>	<b>VLSI DESIGN METHODOLOGIES</b>				<b>9+3</b>
Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.					
<b>UNIT II</b>	<b>DESIGN RULES</b>				<b>9+3</b>
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - Placement and Partitioning - Circuit representation - Placement algorithms – partitioning.					
<b>UNIT III</b>	<b>FLOOR PLANNING</b>				<b>9+3</b>
Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.					
<b>UNIT IV</b>	<b>SIMULATION</b>				<b>9+3</b>
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.					
<b>UNIT V</b>	<b>MODELLING AND SYNTHESIS</b>				<b>9+3</b>
High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.					
		<b>L : 45</b>	<b>T : 0</b>	<b>P : 0</b>	<b>J : 0 Total: 45 PERIODS</b>

## REFERENCES

- 1 S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002
- 2 N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", 3<sup>rd</sup> edition., 2005, Springer International Edition.
- 3 Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
- 4 Rolf Drechsler: "Evolutionary Algorithm for VLSI", second edition.
- 5 Trim burger, "Introduction to CAD for VLSI", Kluwer Academic Publisher, 2002.

## COURSE OUTCOMES

At the end of the course student should be able to:

- CO1** Understand the tools used for automation and graph theory in VLSI design methodologies
- CO2** Infer the techniques used for placement and partitioning in VLSI circuit design
- CO3** Illustrate the floor planning and routing algorithms in VLSI- CAD
- CO4** Apply the simulation techniques in various levels of design abstraction
- CO5** Analyze the types of synthesis tools used to schedule and assign the device modeling.

**.UNIT I                      RANDOM ACCESS MEMORY TECHNOLOGIES****9+3**

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies - Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures- BiCMOS , DRAMs-Soft Error Failures in DRAMs -Application, Specific DRAMs.

**UNIT II                      NONVOLATILE MEMORIES****9+3**

Masked Read-Only Memories (ROMs)-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Read-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

**UNIT III                      MEMORY FAULT MODELING, MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE****9+3**

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

**UNIT IV                      RELIABILITY AND RADIATION EFFECTS****9+3**

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification.

**UNIT V                      PACKAGING TECHNOLOGIES****9+3**

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

**L : 45                      T: 0                      P: 0                      Total: 45 PERIODS****REFERENCES**

- 1 Ashok K.Sharma, "Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of India Private Limited, New Delhi, 2004.
- 2 TegzeP.Haraszti, "CMOS Memory Circuits", Kluwer Academic publishers, 2001.
- 3 Betty Prince, " Emerging Memories: Technologies and Trends", Kluwer Academic publishers, 2002

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the basic concepts of memories.
- CO2** Analysis of Volatile and Non Volatile Memories.
- CO3** Comprehensive understanding of Advanced Memory packaging Technologies.
- CO4** Knowledge about the Advanced VLSI Testing.
- CO5** Idea about the Fault Tolerant Detection

**UNIT I                    DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES**

**9**

Standard Digital Signal Processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

**UNIT II                    DIGITAL SIGNAL PROCESSING**

**9**

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

**UNIT III                    DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS**

**9**

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects.

**UNIT IV                    SYNTHESIS OF DSP ARCHITECTURES**

**9**

Multiprocessors and multicomputer, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

**UNIT V                    ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN**

**9**

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.

**L : 45            T: 0    P: 0    Total: 45 PERIODS**

**REFERENCES**

- 1 A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.
- 2 Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach", Second Edition, Pearson Education, Asia.
- 3 KeshabK.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.
- 4 Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the technologies used to design standard DSP processors
- CO2** Identify the frequency response of DSP by types of Fourier transforms
- CO3** Relate the characteristics of filters in DSP processors and its sampling factors
- CO4** Synthesize the DSP architectures by means of various algorithmic techniques
- CO5** Familiarize the various applications of arithmetic units and accumulator in DSP processors

**16VL607**

**ANALOG VLSI DESIGN**

<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>3</b>	<b>1</b>	<b>0</b>	<b>4</b>

**UNIT I ANALOG CIRCUIT BUILDING BLOCKS**

**9+3**

Switches, active resistors - Current sources and sinks - Current mirrors/amplifiers - Voltage and current references, Comparator, Multiplier.

**UNIT II AMPLIFIERS**

**9+3**

MOS and BJT inverting amplifier - Improving performance of inverting amplifier - CMOS and BJT differential amplifiers - Characterization of Op-Amp - The BJT two stage op-amp - The CMOS two stage op-amp - Op-amps with output stage, Folded Cascode op-amp, Trans conductance Amplifier.

**FILTERS**

Low pass filters - High pass filters – Band Pass filters – Phase Locked Loops.

**UNIT III DATA CONVERTER FUNDAMENTALS**

**9+3**

Ideal A/D and D/A converters, Quantization noise, Signed codes, Performance limitations

**UNIT IV D/A AND A/D CONVERTERS**

**9+3**

D/A converter: Current scaling, Voltage scaling and Charge scaling D/A converters - Serial D/A converters - Serial A/D converters, Parallel - High performance A/D converters.

**UNIT V LAYOUT ISSUES**

**9+3**

CMOS design rules - layout of CMOS - BJT- Capacitors – Resistors - Mixed layout issues: Floor planning, power supply & ground, fully differential matching, Guard rings and shielding.

**L : 45 T: 15 P: 0 Total: 60 PERIODS**

**REFERENCES**

- 1 Randall L Geiger, Phillip E Allen and Noel R Strader, "VLSI Design Techniques for Analog and Digital Circuits", McGraw Hill, International Edition, 1990.
- 2 Jose E Franca HannisTsiividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, International Edition, 2002.
- 3 David A Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 2002.
- 4 Phillip Allen and Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2000.
- 5 Benhard Razavi, "Data Converters", Kluwer Publishers, 2000.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Familiarize the basic blocks of analog circuits and its applications
- CO2** Understand the characteristics of amplifiers and filters used in analog circuits
- CO3** Infer the fundamental design in data converters with its limitations
- CO4** Analyze the performance of serial and parallel type data converters
- CO5** Estimate the performance of Analog chip by CMOS layout design rules

**16VL608****TESTING OF VLSI CIRCUITS**

L	T	P	C
3	1	0	4

**UNIT I                   BASICS OF TESTING AND FAULT MODELING****9+3**

Introduction to testing – Faults in Digital Circuits – Modeling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

**UNIT II                   TEST GENERATION FOR COMBINATIONAL AND  
SEQUENTIAL CIRCUITS****9+3**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

**UNIT III                  DESIGN FOR TESTABILITY****9+3**

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

**UNIT IV                  SELF – TEST AND TEST ALGORITHMS****9+3**

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

**UNIT V                  FAULT DIAGNOSIS****9+3**

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

**L : 45                   T: 15    P: 0    Total: 60 PERIODS****REFERENCES**

- 1 M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
- 2 P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
- 3 M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
- 4 A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1   Able to carry out research and development in the area of testing and verification of VLSI circuits.
- CO2   Apply techniques to improve testability of VLSI circuits.
- CO3   Utilize logic simulation methods, ATPG, BIST and boundary scan techniques in testing of VLSI circuits.
- CO4   Apply functional, timing and formal verification methods at various design abstractions of VLSI circuits
- CO5   Solve practical and state of the art testing and verification problems to serve VLSI industries

**UNIT-I SEMICONDUCTOR PHYSICS****9**

Quantum Mechanical Concepts- Carrier Concentration- Transport Equation- Mobility and Resistivity- Carrier diffusion- Carrier Generation and Recombination- Continuity equation- Tunneling and High field effects- Ideal diode current equation.

**UNIT-II DIODE MODELING****9**

Static, Small signal and Large signal models of PN junction Diode-SPICE model for a Diode- Temperature and Area effects on Diode Model Parameters

**UNIT-III BIPOLAR DEVICE MODELING****9**

Transistor Action-Terminal currents - Switching- Static, Small signal and Large signal Eber-Moll models of BJT- Gummel Poon Model- SPICE modeling - temperature and area effects.

**UNIT-IV MOSFET MODELING****9**

MOS Transistor – NMOS- PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel and Narrow Width Effect- Models for Enhancement- Depletion Type MOSFET- MOS Models in SPICE.

**UNIT-V OPTOELECTRONIC DEVICE MODELING****9**

Static and Dynamic Models - Rate Equations - Numerical Technique - Equivalent Circuits - Modeling of LEDs - Laser Diode and Photo detectors.

**L : 45      T : 0      P : 0      Total: 60 PERIODS**

**REFERENCES**

- 1 KiatSeng Yeo, Samir S.Rofail, Wang-Ling Gob, "CMOS / BiCMOS ULSI – Low Voltage, Low Power", Person education, Low price edition, 2003
- 2 Sze S.M. "Semiconductor Devices - Physics and Technology", John Wiley and sons, 1985.[
- 3 Giuseppe Massobrio and Paolo Antogentti, "Semiconductor Device Modeling with SPICE" Second Edition, McGraw-Hill Inc, New York, 1993
- 4 Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", Pearson Education ASIA, 2<sup>nd</sup> edition, 2000.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Explain the small- and large-signal models of MOS transistors
- CO2** Demonstrate the use of analog circuit analysis techniques to analyze the operation and behavior of various analog integrated circuits.
- CO3** Analyze and design current mirror circuits
- CO4** Analyze and design analog operational transconductance amplifiers
- CO5** Design a two stage open loop comparator

**LIST OF EXPERIMENTS**

1. Modeling of Combinational Digital system using VHDL.
2. Modeling of Combinational Digital system using Verilog.
3. Modeling of Sequential Digital system using VHDL.
4. Modeling of Sequential Digital system using Verilog.
5. Design and Implementation of ALU using FPGA.
6. Simulation of NMOS and CMOS circuits using CADENCE
7. Implementation of MAC Unit using FPGA

**MAJOR EQUIPMENTS / SOFTWARE REQUIRED****Hardware**

- XILINX/ALTERA

**Software**

- Cadence/tanner/mentor graphics

**L : 0 T: 0 P: 30 C: 1 Total:30 PERIODS****COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the combinational circuits modeling in Verilog and VHDL
- CO2** Understand the sequential circuits modeling in Verilog and VHDL
- CO3** Design an ALU and implement by FPGA XILINX/ALTERA
- CO4** simulate and analyze the transient response of NMOS and CMOS using CADENCE
- CO5** Design a MAC and implement by FPGA XILINX/ALTERA

**16VL606**

**INDUSTRIAL TRAINING -I**

**L    T    P    C**

**0    0    2    1**

Minimum of two weeks in an Industry in the area of Electronics and communication Engineering. The industrial training should give exposure to the practical aspects of the discipline. In addition, the student may also work on a specified task or project which may be assigned to him/her. The outcome of the industrial training should be presented in the form of a report.

**Total: 2 Weeks**



**LIST OF EXPERIMENTS**

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD.
3. Design and Implementation of the following adders using FPGA
  - Ripple carry adder
  - Carry save adder
  - Carry look ahead adder
  - Carry bypass adder
  - Carry select adder
4. Design and Implementation of the following multiplier using FPGA.
  - Array multiplier
  - Booth multiplier
  - Wallace multiplier
  - Baugh wooley multiplier
5. Simulation of the following circuits using CADENCE
  - Transmission gate
  - Pass transistor logic(NAND,NOR)
  - Domino logic (NAND,NOR)
  - D latch
  - Current mirror
  - Differential pair
6. Design and Implementation of the following adders using CADENCE  
Full adder(8T,10T,12T,16T)

**MAJOR EQUIPMENTS / SOFTWARE REQUIRED****Hardware**

- XILINX/ALTERA

**Software**

- Cadence/tanner/mentor graphics

**L : 0    T : 0    P : 60    J : 0    C : 2    Total:60 PERIODS**

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the concepts of ALU and Processor and design using XILINX/ALTERA
- CO2** Design and implement the types of adders using FPGA
- CO3** Design and implement the types of Multipliers using FPGA
- CO4** Analyze and evaluate the performance of dynamic digital circuits using CADENCE
- CO5** Evaluate the transient response of NMOS and CMOS level adders using CADENCE

**16VL611**

**INDUSTRIAL TRAINING -II**

**L    T    P    C**

**0    0    2    1**

Minimum of two weeks in an Industry in the area of Electronics and communication Engineering. The industrial training should give exposure to the practical aspects of the discipline. In addition, the student may also work on a specified task or project which may be assigned to him/her. The outcome of the industrial training should be presented in the form of a report.

**Total: 2 Weeks**

**UNIT I DEFINING THE RESEARCH PROBLEM**

Formulation of research problem; Identification and selection of problem. Meaning purpose and principles of research design. Design criteria-different types of research and Experimental design. Purpose of the study: Exploratory, Descriptive, Hypothesis Testing.

**UNIT II METHODS OF DATA COLLECTION**

Sources of data- methods of data collection- observation, questionnaire, interview, schedules and interviews. Sampling Techniques – Probabilistic and non-probabilistic samples. Issues of Precision and Confidence in determining Sample Size. Hypothesis testing, Parametric and Non-Parametric (Chi-square, Kolmogorov - Simronov, Mann-Whitney (U test), Kriskal Wallis( H Test).

**UNIT III MEASUREMENT AND SCALING TECHNIQUES**

Measurement in research- measurement in scales- scaling techniques, Thurstone V scale Model, Os goods semantic, Likert type, Q sort and Multi-Dimensional , scale constitution techniques- content analysis. Processing and analysis of data-processing operation- problem in processing, types of analysis.

**UNIT IV MULTI VARIATE ANALYSIS TECHNIQUES**

Mobile Databases: Location and Handoff Management - Effect of Mobility on Data Management - Location Dependent Data Distribution - Mobile Transaction Models - Concurrency Control - Transaction Commit Protocols- Mobile Database Recovery Schemes

**UNIT V INTERPRETATION AND REPORT WRITING**

Meaning and techniques of interpretation, significance of report writing, different types of steps in report writing, case studies.

**L : 0 T: 0 P: 30 Total: 30 PERIODS**

**REFERENCES**

- 1 Kothari C.R., “Research Methodology Methods and Techniques”, New Age International Publishers, 2006.
- 2 Pannerselvam R., ”Research Methodology”, PHI Learning Ltd, 2004.
- 3 Kidder L.H., “Research Methods in Social Relations”, Hall Saunders International, 2002.
- 4 Sedhu A.M., & Singh A., “Research Methodology in Social Science”, Himalaya Publishing House, Mumbai, 2003.

**COURSE OUTCOMES**

**At the end of the course student should be able to:**

- CO1** Understand the importance of research problem framing
- CO2** Infer the techniques used for data collection
- CO3** Illustrate the measurement and scaling techniques of research methodology
- CO4** Apply the multivariate analysis tetchiness in research problem selection
- CO5** Analyze the types of report writing.

**16VL702**

**Project Work - Phase I**

<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>0</b>	<b>0</b>	<b>12</b>	<b>6</b>

1. Identification of a real life problem in thrust areas
2. Developing a mathematical model for solving the above problem
3. Finalization of system requirements and specification
4. Proposing different solutions for the problem based on literature survey
5. Future trends in providing alternate solutions
6. Consolidated report preparation of the above

**L : 0      T: 0    P: 180    Total: 180 PERIODS**

**16VL703**

**PROJECT PHASE – II**

<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
<b>0</b>	<b>0</b>	<b>24</b>	<b>12</b>

**The project involves the following:**

Preparing a project - brief proposal including

1. Problem identification
2. A statement of system / process specifications proposed to be developed (block diagram / concept tree)
3. List of possible solutions including alternatives and constraints
4. Cost benefit analysis
5. Time line of activities

**A report highlighting the design finalization [based on functional requirements & standards (if any)]**

A presentation including the following:

1. Implementation phase (hardware / software / both)
2. Testing & validation of the developed system
3. Learning in the Project
4. Consolidated report preparation

**L: 0 T: 0 P: 360 TOTAL : 360 PERIODS**

<b>16VL612</b>	<b>RECONFIGURABLE COMPUTING</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>	
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>	
<b>UNIT-I</b>	<b>DEVICE ARCHITECTURE</b>					<b>9</b>
General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs– Device Architecture - Case Studies.						
<b>UNIT-II</b>	<b>RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS</b>					<b>9</b>
Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.						
<b>UNIT-III</b>	<b>PROGRAMMING RECONFIGURABLE SYSTEMS</b>					<b>9</b>
Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing						
<b>UNIT-IV</b>	<b>MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS</b>					<b>9</b>
The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bitstream Generation – Case Studies with Appropriate Tools.						
<b>UNIT-V</b>	<b>APPLICATION DEVELOPMENT WITH FPGA</b>					<b>9</b>
Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs.						

**L : 45      T: 0    P: 0    Total: 60 PERIODS**

## REFERENCES

- 1 Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
- 2 Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation”, Elsevier / Morgan Kaufmann, 2008.
- 3 Christophe Bobda, “Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications”, Springer, 2010

## COURSE OUTCOMES

At the end of the course student should be able to:

- CO1** Compare the architecture of general purpose and reconfigurable CPLD and fpgas
- CO2** Understand the reconfigurable computing systems with real time applications
- CO3** Model and compute the FPGA applications in reconfigurable architectures
- CO4** Develop mapping designs by routing and floor plan for reconfigurable architectures.
- CO5** Apply the reconfigurable computations with FPGA in soc design

<b>16VL613</b>	<b>VLSI ARCHITECTURE FOR IMAGE AND VIDEO PROCESSING</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>
<b>UNIT-I</b>	<b>IMAGE PROCESSING ALGORITHMS</b>				<b>9</b>
Introduction – Image Processing Tasks- Low level Image Processing Operations – Description of some intermediate level operations –Requirements for Image processor architecture.					
<b>UNIT-II</b>	<b>IMAGE PROCESSING ARCHITECTURES AND PIPELINED LOW LEVEL IMAGE PROCESSING</b>				<b>9</b>
Classification of Architectures – Uni and Multi processors – MIMD systems – SIMD systems – Pipelines – Devices for cellular logic processing – Design aspects of real time low level image processors –Design method for special architectures.					
<b>UNIT-III</b>	<b>PIPELINED ARCHITECTURES &amp; 2D AND 3D IMAGE PROCESSING ARCHITECTURES</b>				<b>9</b>
Architecture of a cellular logic processing element – Second decomposition in datapath and control – Real time pipeline for low level image processing – Design aspects of Image Processing architectures – Implementation of Low level 2D and 3D and Intermediate level algorithms.					
<b>UNIT-IV</b>	<b>VIDEO PROCESSING ALGORITHMS</b>				<b>9</b>
Motion Estimation Algorithms – Complexity Analysis Methodology –Complexity analysis of MPEG – 4 Visual – Analysis of Fast Motion Estimation Algorithms.					
<b>UNIT-V</b>	<b>VLSI ARCHITECTURES FOR VIDEO PROCESSING</b>				<b>9</b>
General design space evaluation – Design space motion estimation architectures – Motion estimation architectures for MPEG-4 – Design Trade offs – VLSI Implementation search engine I and Search engine II.					

**L : 45                      T: 0    P: 0    Total: 60 PERIODS**

#### **REFERENCES**

- 1 Peter M. Kuhn, —Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation ", Springer ISBN 978-1-4419-5088-8, First Edition, 2010
- 2 Pieter Jonker, —Morphological Image Processing: Architecture and VLSI design, Springer. ISBN: 9020127667, First Edition, 1992
- 3 Rafael C. Gonzalez & Richard E. Woods, —Digital Image Processing, Prentice Hall; Third edition, 2007
- 4 A.MuratTekalp, —Digital Video Processing, Pearson Education, Noida, First Edition, 2010.

#### **COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Analyze the algorithms and operations of VLSI image processors
- CO2** Classify the types of image processing architectures and its design methodologies
- CO3** Infer the functions of pipelined, 2D and 3D algorithms in image processors
- CO4** Estimate the complexity of video processing by motion estimation algorithms
- CO5** Understand the design tradeoff of videos using VLSI architecture

<b>16VL614</b>	<b>HARDWARE DESCRIPTION LANGUAGE</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

**UNIT-I BASIC CONCEPTS OF HARDWARE DESCRIPTION LANGUAGE 9**

Comparison between HDL and High Level Language Hierarchy, Concurrency, Logic and Delay Modeling, Structural, Data flow, Behavioral Styles of Hardware Description, Architecture of event driven simulation.

**UNIT-II VHDL 9**

Data Types, Operators, Classes of Objects, entities and architectures , Attributes – concurrent statements- sequential statements- signals and variables- Behavior, dataflow and structural modeling- Configurations, functions- procedures- packages - test benches- Design Example

**UNIT-III VERILOG 9**

Signals, Identifier Names, Net and Variable Types, operators, Gate instantiations, Verilog module, concurrent and procedural statements, UDP, sub circuit parameters, function and task, -test benches- Design Examples.

**UNIT-IV TIMING ISSUES 9**

Modeling delay, Timing Modeling, Timing Assertion, Setup and hold times for clocked devices.

**UNIT-V SYSTEM MODELLING 9**

Processor model, RAM model, UART Model, Interrupt Controller

**L : 45 T: 0 P: 0 Total: 60 PERIODS**

**REFERENCES**

- 1 Bhasker J, "A VHDL Primer", Prentice Hall, 1999.
- 2 Michael D Ciletti, "Advanced Digital Design with Verilog HDL", Pearson education, 2005
- 3 Douglass Perry, "VHDL", Tata McGraw Hill, McGraw-Hill Professional, 4<sup>th</sup> Edition, May 2002.
- 4 Volnei A Pedroni, "Circuit Design with VHDL", Prentice Hall, 2004
- 5 Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall NJ, USA, 2003.
- 6 Neil Weste and Kamran Eshraghian "Principles of CMOS VLSI Design", Addison Wesley, 2000

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the fundamentals and various levels of abstractions in HDL
- CO2** Familiarize the basic concepts of VHDL and test benches with design examples
- CO3** Infer the basic concepts of Verilog and test benches with design examples
- CO4** Analyze the timing issues of clocked devices in digital logic circuits.
- CO5** Model a system using Verilog/VHDL and estimate its performance.



**UNIT-I DEEP SUBMICRON DIGITAL IC DESIGN, TRANSISTORS AND DEVICES MOS AND BIPOLAR, FABRICATION, LAYOUT AND SIMULATION 9**

Review of Digital Logic Gate Design-digital IC design-computer Aided Design of digital circuits-The MOS Transistor-Bipolar Transistor and circuits-IC Fabrication technology Layout basics-modeling the MOS transistor for circuit simulation-SPICE MOS level1 device model-BSIM3 model-additional effects in MOS transistors-SOI technology.

**UNIT II MOS INVERTER CIRCUITS, STATIC MOS GATE CIRCUITS 9**

Voltage transfer characteristics-noise margin definitions-resistive load inverter design NMOS transistors as load devices-CMOS inverter-pseudo-NMOS inverters-sizing inverters- tristate inverters-CMOS gate circuits-complex CMOS gates-XOR and XNOR gates-multiplexer circuits – Flip-flops and latches – D flip flops and latches – power dissipation in CMOS gates-power and delay trade-offs.

**UNIT III HIGH SPEED CMOS LOGIC DESIGN, TRANSFER GATE AND DYNAMIC LOGIC DESIGN 9**

Switching time analysis – detailed load capacitance calculation – improving delay calculation with input slope - gate sizing for optimal path delay – optimizing path with logical effort – basic concepts of transfer gate – CMOS transmission gate logic – dynamic D latches and D flip-flops – domino logic –voltage bootstrapping.

**UNIT IV SEMICONDUCTOR MEMORY DESIGN, ADDITIONAL TOPICS IN MEMORY DESIGN, INTERCONNECT DESIGN 9**

Introduction-MOS decoders – static RAM cell design-SRAM column I/O circuitry –memory architecture content addressable memories-FPGA-dynamic Read-Write memories-Read Only memories-EEPROMs and E2PROMs-flash memory-FRAMs interconnect RC delays-buffer insertion for very long wires-interconnect coupling capacitance-interconnect inductance-antenna effects.

**UNIT POWER GRID AND CLOCK DESIGN, LOW POWER CMOS LOGIC CIRCUITS, CHIP INPUT AND OUTPUT CIRCUITS, DESIGN FOR TESTABILITY 9**

Power distribution design-clocking and timing issues, phase-locked loops/delay-locked loops – low power design through voltage scaling – estimation and optimization of switching activity – reduction of switched capacitance – adiabatic logic circuits – ESD protection – input circuits – output circuits and L(di/dt) noise– on-chip clock generation and distribution – latch-ups and its prevention – fault types and models –controllability and observability – adhoc testable design techniques – scan based techniques – Built-In-Self Test(BIST) techniques – current monitoring IDDQ test.

**L : 45 T: 0 P: 0 Total: 60 PERIODS**

**REFERENCES**

- 1 David A Hodges, Horace G Jackson, Resve A Saleh, “Analysis and design of Digital Integrated Circuits – in deep submicron technology”, Tata McGraw Hill, Edition-2005
- 2 Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits-analysis and design”, Tata McGraw Hill, Third edition-2003.
- 3 Uyemura, Chip design of Submicron VLSI: CMOS Layout and Simulation, Thomson Engineering, 2005.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Relate various models and simulators to design digital ics
- CO2** Understand the fundamental concepts of high speed CMOS and dynamic logic design.
- CO3** Analyze the switching time and optimization of dynamic logic design
- CO4** Familiarize the RAM and ROM memory devices used for interconnect design.
- CO5** Estimate the delay by pipelining,clock,timing issues and testability of faulty circuits.

**UNIT-I EMBEDDED ARCHITECTURE****9**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded System Design, Embedded System Design Process - Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration.

**UNIT-II EMBEDDED PROCESSOR AND COMPUTING PLATFORM****9**

ARM Embedded Systems, ARM Processor Fundamentals –ARM organization and implementation – ARM CPU cores, ARM support for system development-ARM support for Operating Systems

**UNIT-III REAL-TIME OPERATING SYSTEM CONCEPTS****9**

Embedded and Real-Time Systems-Introduction to Real-Time Operating Systems-Brief history of operating systems-Defining an RTOS-The Scheduler-Objects-Services-Key Characteristics of an RTOS-System using RTOS-RTOS concepts and definitions-RTOS building blocks for system development

**UNIT-IV EMBEDDED SYSTEM DESIGN USING MSP430****9**

Introduction- Architecture: CPU and Memory-Hardware considerations- Instruction set-Flash memory- Functions, Interrupts and Low power modes-Timers-Analog input and output.

**UNIT-V EMBEDDED NETWORKS****9**

Distributed Embedded Architecture - Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link ports, Ethernet, Myrinet, Internet. Design Example: Elevator Controller.

**L : 45      T: 0    P: 0    Total: 60 PERIODS****REFERENCES**

- 1 David A Hodges, Horace G Jackson, Resve A Saleh, "Analysis and design of Digital Integrated Circuits – in deep submicron technology", Tata McGraw Hill, Edition-2005
- 2 Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits-analysis and design", Tata McGraw Hill, Third edition-2003.
- 3 Uyemura, Chip design of Submicron VLSI: CMOS Layout and Simulation, Thomson Engineering, 2005.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand basic concept of embedded systems.
- CO2** Apply and analyze the applications in various processors and domains of embedded system.
- CO3** Analyze and develop embedded hardware and software development cycles and tools
- CO4** Analyze to understand what a microcomputer, core of the embedded system.
- CO5** Remember the definitions of embedded networks

<b>16VL617</b>	<b>DESIGNING WITH CPLD &amp; FPGA</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>
<b>UNIT I</b>	<b>OVERVIEW OF VLSI DESIGN METHODOLOGY</b>				<b>9</b>
VLSI design process - Architectural design - Logical design - Physical design - Layout styles - Fullcustom, Semicustom approaches.					
<b>UNIT II</b>	<b>COMBINATIONAL CIRCUITS</b>				<b>9</b>
Shannon's expansion theorem - Design using Multiplexers, Decoders - Design of static hazard free and dynamic hazard free logic circuits					
<b>UNIT III</b>	<b>SEQUENTIAL CIRCUITS</b>				<b>9</b>
Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards- Unger's theorem.					
<b>UNIT IV</b>	<b>PROGRAMMABLE LOGIC DEVICES</b>				<b>9</b>
Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Design of state machine using Algorithmic State Machines (ASM) chart as a design tool.					
<b>UNIT V</b>	<b>CPLDS AND FPGAS</b>				<b>9</b>
Architectures of CPLDs and FPGAs.- Design of combinational and sequential circuits using CPLDs and FPGAs- Design examples					
		<b>L : 45</b>	<b>T : 0</b>	<b>P : 0</b>	<b>Total: 45 PERIODS</b>

## REFERENCES

- 1 Charles H Roth, "Digital system Design with VHDL", Thomson, 1998.
- 2 James E Palmer and David E Perlman, "Introduction to Digital Systems ", Tata McGraw Hill, 1996.
- 3 Robert Dueck, "Digital design with CPLD applications and VHDL", Thomson, 2004.
- 4 Bob Zeidman, "Designing with CPLDs and FPGAs", CMP, 2002.

## COURSE OUTCOMES

At the end of the course student should be able to:

- CO1** understand the fundamental concepts of VLSI design process and methodology
- CO2** Analyze and design hazard free combinational circuits with theorems
- CO3** Analyze and design hazard free sequential circuits with theorems
- CO4** Infer the types and functions of Programmable Logic devices
- CO5** Examine the architecture of CPLD and FPGA with examples

**UNIT-I VLSI AND ITS FABRICATION****9**

Introduction, IC manufacturing, CMOS technology, IC design techniques, IP based design, Fabrication process-Transistors, Wires and Via, Fabrication Theory reliability, Layout Design and tools.

**UNIT-II COMBINATIONAL LOGIC NETWORKS****9**

Logic Gates: Combinational Logic Functions, Static Complementary Gates, Switch Logic, Alternate Gate circuits, Low power gates, Delay, Yield, Gates as IP, Combinational Logic Networks-Standard Cell based Layout, Combinational network delay, Logic and Interconnect design, Power optimization, Switch logic network, logic testing;

**UNIT-III SUBSYSTEM DESIGN****9**

Sequential Machine-Latch and Flip flop, System design and Clocking, Performance analysis, power optimization, Design validation and testing; Subsystem Design-Combinational Shifter, Arithmetic Circuits, High Density memory, Image Sensors, FPGA, PLA, Buses and NoC, Data paths, Subsystems as IP..

**UNIT-IV FLOOR PLANNING AND ARCHITECTURE DESIGN****9**

Floor planning-Floor planning methods, Global Interconnect, Floor plan design, Off-chip Connections Architecture Design- HDL, Register-Transfer Design, Pipelining, High Level Synthesis, Architecture for Low power, GALS systems, Architecture Testing, IP Components, Design Methodologies, Multiprocessor System-on-chip Design.

**UNIT-V DESIGN SECURITY****9**

IP in reuse based design, Constrained based IP protection, Protection of data and Privacy constrained based watermarking for VLSI IP based protection

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 Wayne wolf, "Modern VLSI Design:IP-based Design", Pearson Education,2009.
- 2 Qu gang, "Intellectual Property Protection in VLSI Designs: Theory and Practice", kluwer academic publishers,2003

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Relate the basic concepts of IC fabrication techniques with layout design and tools
- CO2** Analyze the delay and power optimization in combinational logic networks.
- CO3** estimate the clocking issues and system performance of sequential logic and its subsystems
- CO4** Infer the methods of floor plan and low power design methodologies in MultiprocessorSoC
- CO5** classify the types of IP based protection techniques for VLSI design security

**UNIT I INTRODUCTION TO PROCESSOR DESIGN****9**

Abstraction in hardware design- MUO – a simple processor – Processor Design trade off- Design for low power consumption.

ARM ARCHITECTURE: Acorn RISC Machine – Architecture Inheritance – ARM Programming Model- ARM Development Tools – 3 and 5 Stage Pipeline ARM Organization - ARM Instruction Execution and Implementation – ARM Co-Processor Interface.

**UNIT II ARM ASSEMBLY LANGUAGE PROGRAMMING****9**

ARM Instruction Types – Data Transfer, Data Processing and Control Flow Instructions - ARM Instruction Set – Co-Processor Instructions.

**UNIT III ARCHITECTURAL SUPPORT FOR HIGH LEVEL LANGUAGE****9**

Data Types – Abstraction in software Design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory.

MEMORY HIERARCHY: Memory Size and Speed – On Chip Memory – Caches – Cache Design – an Example- Memory management.

**UNIT IV ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT****9**

Advanced Microcontroller Bus Architecture – ARM Memory Interface – ARM Reference Peripheral Specification – Hardware System Prototyping Tools – Emulator – Debug Architecture.

**UNIT V ARCHITECTURAL SUPPORT FOR OPERATING SYSTEM****9**

An Introduction to Operating Systems – ARM System Control Coprocessor- CP15 Protection Unit Registers – ARM Protection Unit – CP15 MMU Registers – ARM MMU Architecture – Synchronization – Context Switching Input and Output.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 Steve Furber, “ARM System on Chip Architecture”, Addison- Wesley Professional, 2<sup>nd</sup> Edition, Aug 2000
- 2 Ricardo Reis “Design of System on a Chip: Devices and Components” Springer, 1<sup>st</sup> Edition, July 2004.
- 3 Jason Andrews “Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)” Newnes, BK and CD-ROM (Aug 2004).
- 4 Rashinkar P, Paterson and Singh L, “System on a Chip Verification – Methodologies and Techniques”, Kluwer Academic Publishers, 2001.
- 5 System on chip verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001 Kluwer Academic Publishers.

**COURSE OUTCOMES**

At the end of the course student should be able to:

**CO1** Demonstrate the abstraction in Hardware, SOC of ARM Processor

**CO2** Evaluate and analyze system on chip RISC Machine, three and five stage Pipeline

**CO3** Explain Memory Design for SOC

**CO4** Develop the Interconnect Customization and Configuration

**CO5** Explain the SOC design approaches and AES algorithm

**UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs****9**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs– Multiple access memory – Multi-port memory – VLIW architecture- Pipelining –Special Addressing modes in P-DSPs – On chip Peripherals.

**UNIT II TMS320C5X PROCESSOR****9**

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Simple programs-Application Programs for processing real time signals.

**UNIT III TMS320C3X PROCESSOR****9**

Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

**UNIT IV ADSP PROCESSORS****9**

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

**UNIT V ADVANCED PROCESSORS****9**

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications” – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
- 2 User guides Texas Instrumentation, Analog Devices, Motorola.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** understand the fundamental concepts of various programmable DSPs
- CO2** infer the characteristics and operations of TMS-5X processors.
- CO3** understand the functions and operations of TMS-3X processors.
- CO4** analyze the performance and characteristics of ADSP
- CO5** compare the performance of various advanced DSP and applications.

**UNIT-I PERFORMANCE PARAMETERS OF RF CIRCUITS****9**

Gain Parameters, Non-linearity parameters, Noise figure, Phase Noise, Dynamic range, RF front end performance parameters, performance trade offs in an RF circuit.

**UNIT-II FILTER DESIGN****9**

Modern filter design, Frequency and impedance scaling, High Pass filter design, Band pass filter design, Band reject filter design, the effects of finite Q.

**UNIT-III HIGH FREQUENCY AMPLIFIER DESIGN****9**

Zeros as Bandwidth enhances, Shunt-series Amplifier, Bandwidth enhancement with frequency Doublers, Tuned amplifiers, Neutralization and unilateralization, cascaded Amplifiers, LNA Topologies.

**UNIT-IV MIXERS AND OSCILLATORS****9**

Mixer fundamentals, Non linear systems as Linear mixers, multiplier based mixers, Sub sampling mixers. Problems with purely linear oscillators, Tuned oscillator, Negative Resistance oscillators, frequency synthesis. .

**UNIT-V RF POWER AMPLIFIERS****9**

General considerations, Class A, AB, B & C Power amplifier, Class D, E & F amplifiers, modulation of power amplifiers, RF Power amplifier design examples.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 Aleksandar Tasic, Wouter.A.Serdijn, John.R.Long, "Adaptive Low Power Circuits for Wireless Communication (Analog Circuits and Signal Processing)", Springer, 1<sup>st</sup> Edition, 2006
- 2 Chris Bowick, "RF Circuit design", Newnes (An imprint of Elsevier Science), 1<sup>st</sup> Edition, 1997.
- 3 Thomas.H. Lee, "The design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd Edition, 2004. John Wiley and Sons, 2001.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Estimate various performance parameters of RF circuits
- CO2** Design a filter with better quality factor in high frequency devices
- CO3** Understand various types of high frequency amplifiers used in RF design
- CO4** Familiarize the concepts of mixers and oscillators based on applications
- CO5** Infer the types of Power amplifiers and its characteristics.



**UNIT-I WIRELESS COMMUNICATION BASICS****9**

Digital communication systems- minimum bandwidth requirement, the Shanon limit- overview of modulation schemes- classical channel- wireless channel description- path loss- multipath fading- basics of spread spectrum and spread spectrum techniques- PN sequence.

**UNIT-II TRANSCEIVER ARCHITECTURE****9**

Transceiver design constraints- baseband subsystem design- RF subsystem design- Super heterodyne receiver and direct conversion receiver- Receiver front-end- filter design- non-idealities and design parameters- derivation of noise figure and IP3 of receiver front end.

**UNIT-III LOW POWER DESIGN TECHNIQUES****9**

Source of power dissipation- estimation of power dissipation- reducing power dissipation at device and circuit levels- low voltage and low power operation- reducing power dissipation at architecture and algorithm levels.

**UNIT-IV WIRELESS CIRCUITS****9**

VLSI Design of LNA-wideband and narrow band-impedance matching. Automatic Gain Control(AGC) amplifier-power amplifier- Active mixer- analysis, conversion gain, distortion analysis- low frequency and high frequency case, noise. Passive mixer- sampling mixer and switching mixer- analysis of distortion, conversion gain and noise in these mixers.

**UNIT-V VLSI DESIGN OF SYNTHESIZERS****9**

VLSI design of Frequency Synthesizers (FS) – Parameters of FS - PLL based frequency synthesizer, phase detector/charge pump- dividers- VCO- LC oscillators- ring oscillator- phase noise- loop filter- description, design approaches.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 Bosco Leung, VLSI for Wireless Communication, Springer, 2011.
- 2 Elmad N Farag and Mohamed I Elmasry, Mixed Signal VLSI Wireless Design-Circuits and Systems, Kluwer Academic Publishers, 2002.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the basic concepts wireless communication basics
- CO2** Familiarize different types transceiver architecture
- CO3** Infer the need of low power design techniques
- CO4** Relate the wireless circuits with low power vlsi design circuits
- CO5** Develop the digital signature chip for security using various security algorithms



**UNIT-I BASICS OF NANOELECTRONICS****9**

Basics of nano electronics – capabilities of nano electronics – physical fundamentals of nano electronics – basics of information theory – the tools for micro and nano fabrication – basics of lithographic techniques for nano electronics

**UNIT-II QUANTUM ELECTRON DEVICES****9**

Quantum electron devices – from classical to quantum physics: upcoming electronic devices – electrons in mesoscopic structure – short channel MOS transistor – split gate transistor – Electron wave transistor – Electron spin transistor – quantum cellular automate – quantum dot array – Principles of Single Electron Transistor (SET) – SET circuit design – comparison between FET and SET circuit design.

**UNIT-III NANOELECTRONICS WITH TUNNELING DEVICES AND SUPERCONDUCTING DEVICES****9**

Nanoelectronics with tunneling devices and superconducting devices – tunneling element technology - RTD: circuit design – Defect tolerant circuits - Molecular electronics – elementary circuits – flux quantum devices – application of Superconducting devices – Nanotubes based sensors, fluid flow, gas, temperature, Strain – oxide nanowire, gas sensing (ZnO, TiO, SnO, WO), LPG sensor (SnO powder)- Nano 2 2 3 2 designs and Nanocontacts - metallic nanostructures.

**UNIT-IV SURVEY ON NANOTECHNOLOGY****9**

A survey about the limits – Replacement Technologies – Energy and Heat dissipation – Parameter spread as Limiting Effect – Limits due to thermal particle motion – Reliability as limiting factor – Physical limits – Final objectives of integrated chip and systems.

**UNIT-V MEMORY DEVICES AND SENSORS****9**

Memory devices and sensors – Nano ferroelectrics – Ferroelectric random access memory – Fe-RAM circuit design – ferroelectric thin film properties and integration – calorimetric sensors – electrochemical cells – surface and bulk acoustic devices – gas sensitive FETs – resistive semiconductor gas sensors –electronic noses – identification of hazardous solvents and gases – semiconductor sensor array.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 K.Goser, P.Glosekotter & J.Dienstuhl, “Nanoelectronic and Nanosystems – From Transistors to Molecular Quantum Devices” Springer, 2004
- 2 Rainer Waser, “Nanoelectronics and Information Technology: Advanced Electronic Materials Novel and Devices” Wiley VCH, 2005.
- 3 Mick Wilson, KamaliKannangara, Geoff smith, “Nanotechnology: Basic Science and Emerging Technologies”, Overseas press, 2005.
- 4 W.R. Fahrner, “Nanotechnology and Nanoelectronics: Materials, Devices, Measurement Techniques”, Springer, 2010.
- 5 Branda Paz, “A Handbook on Nanoelectronics”, Vedams books, 2008.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the fundamental concepts of nano electronics and its fabrication techniques
- CO2** Infer the types of quantum electronic devices and its principles of operation.
- CO3** Classify the nano electronics with tunneling devices and superconducting devices with its applications
- CO4** Examine the physical and reliability limitations of nano electronic devices
- CO5** Familiarize the properties and characteristics of nano memory device and sensors

**UNIT-I BASIC CONCEPTS****9**

Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS, Targets: Hardware, Software, Data communication procedures. Threats to Security: Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security.

**UNIT-II ENCRYPTION TECHNIQUES****9**

Conventional techniques, Modern techniques, DES, DES chaining+, Triple DES, RSA algorithm, Key management. Message Authentication and Hash Algorithm: Authentication requirements and functions secure Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service

**UNIT-III FIREWALLS AND CYBER LAWS****9**

Firewalls, Design Principles, Trusted systems, IT act and cyber laws, Virtual private network.

**UNIT-IV FUTURE THREATS TO NETWORK****9**

Recent attacks on networks, VLSI Based Case study

**UNIT-V CRYPTO CHIP DESIGN****9**

VLSI Implementation of AES algorithm. Implementation of DES, IDEA AES algorithm, Development of digital signature chip using RSA algorithm.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 William Stalling "Cryptography and Network Security" Pearson Education, 2005
- 2 Charels P. Pfleeger "Security in Computing" Prentice Hall, 2006
- 3 Jeff Crume "Inside Internet Security" Addison Wesley, 2000.6

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the basic concepts of threats, monitoring control and security systems
- CO2** Familiarize the encryption techniques and algorithm used for message authentication
- CO3** Infer the need of trusted systems, cyber laws and firewall in VPN
- CO4** Relate the recent attacks and threats in VLSI networks with real time examples.
- CO5** Develop the digital signature chip for security using various security algorithms

**UNIT-I INTRODUCTION TO ASICs, CMOS LOGIC, ASIC LIBRARY DESIGN 9**

Types of ASICs - Design flow – CMOS transistors- CMOS Design rules –Combinational logic Cell Sequential logic cell - Transistor as Resistors - Transistor parasitic capacitance – Logical effort - Library cell design – Library architecture

**UNIT-II PROGRAMMABLE ASICs, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9**

Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Xilinx I/O blocks.

**UNIT-III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9**

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Low level design language - PLA tools EDIF- CFI design representation.

**UNIT-IV SILICON ON CHIP DESIGN 9**

Voice over IP SOC - Intellectual Property – SOC Design challenges- Methodology and design- FPGA to ASIC conversion – Design for integration-SOC verification -Set top box SO.

**UNIT-V PHYSICAL AND LOW POWER DESIGN 9**

Over view of physical design flow- tips and guideline for physical design- modern physical design techniques- power dissipation-low power design techniques and methodologies-low power design tools- tips and guideline for low power design.

**L : 45 T: 0 P: 0 Total: 45 PERIODS**

**REFERENCES**

- 1 M.J.S. Smith, Application Specific Integrated Circuits, Pearson Education, 2008.
- 2 FarzadNekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
- 3 Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2009.
- 4 Rajsuman, System-on-a-Chip Design and Test, Santa Clara, CA: Artech House Publishers, 2000.
- 5 F.Nekoogar, Timing Verification of Application-Specific Integrated Circuits (ASICs), Prentice Hall PTR, 1999.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Classify the types of asics and the ASIC library design
- CO2** Relate the PROM technologies in Xilinx and Altera FPGA market.
- CO3** Understand the concepts of ASIC interconnects and software used in PLA design
- CO4** Evaluate the SOC design challenges and design for integration in applications
- CO5** Model a low power circuit with satisfied physical design

3 0 0 3  
9**UNIT-I FUNDAMENTALS**

The importance of signal integrity-new realm of bus design-Electromagnetic fundamentals for signal integrity-max well equations common vector operators-wave propagations-Electro statics-magneto statics-Power flow and the poynting vector-Reflections of electromagnetic waves

**UNIT-II CROSS TALK**

9

Introduction -mutual inductance and capacitance-coupled wave equation-coupled line analysis modal analysis-cross talk minimization signal propagation in unbounded conductive media-classic conductor model for transmission model

**UNIT-III DI-ELECTRIC MATERIALS**

9

Polarization of Dielectric-Classification of Di electric material-frequency dependent di electric material- Classification of Di electric material fiber-Weave effect-Environmental variation in dielectric behavior Transmission line parameters for loosy dielectric and realistic conductors

**UNIT-IV DIFFERENTIAL SIGNALING**

9

Removal of common mode noise-Differential Cross talk-Virtual reference plane-propagation of model voltages common terminology-drawbacks of Differential signaling.

**UNIT-V PHYSICAL TRANSMISSION LINE MODEL**

9

Introduction- non ideal return paths-Vias-IO design consideration-Push-pull transmitter-CMOS receivers-ESSD protection circuits-On chip Termination

**L : 45 T: 0 P: 0 Total: 45 PERIODS****REFERENCES**

- 1 Advanced Signal Integrity for High-Speed Digital Designs By Stephen H. Hall, Howard L. Heck
- 2 Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS by James Edgar Buchanan

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the fundamentals of signal integrity for high speed devices
- CO2** Analyze the crosstalk in inductive and capacitive modeled high speed devices
- CO3** Estimate the behavior of dielectric materials and its characteristics
- CO4** Infer the differential signal techniques used in high speed devices
- CO5** Illustrate the concepts physical transmission model by push-pull transmitter and receivers

**UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION 9**

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

**UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING 9**

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments

**UNIT III DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION 9**

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Fick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

**UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION 9**

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

**UNIT V ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES 9**

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – packaging design consideration – VLSI assembly technology – Package fabrication technology

**L : 45 T: 0 P: 0 Total: 45 PERIODS**

**REFERENCES**

- 1 S.M.Sze, "VLSI Technology", Mc.Graw.Hill Second Edition. 2002.
- 2 Douglas A. Pucknell and Kamran Eshraghian, "Basic VLSI Design", Prentice Hall India. 2003.
- 3 Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design", Prentice Hall India.2000.
- 4 Wayne Wolf,"Modern VLSI Design", Prentice Hall India.1998.
- 5 Essentials of VLSI circuits and Systems, K.Eshraghian ,Eshraghian.D, A.Pucknell, 2005, PHI

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the techniques used for IC fabrication.
- CO2** Infer the methods of etching and lithography for IC fabrication
- CO3** Relate various methods of oxidation, diffusion and implantation techniques.
- CO4** Apply the integration and simulation process of IC fabrication
- CO5** Explain the assembly and packaging techniques in IC fabrication.

**UNIT I INTRODUCTION TO VLSI TECHNOLOGY**

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

**UNIT II PLACEMENT USING TOP-DOWN APPROACH**

9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic-Ratio cut-partition with capacity and i/o constraints. Floor planning: Rectangular dual floor planning-hierarchical approach- simulated annealing- Floor plan sizing.

Placement: Cost function- force directed method- placement by simulated annealing-partitioning placement- module placement on a resistive network – regular placement-linear placement.

**UNIT III ROUTING USING TOP DOWN APPROACH**

9

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches-hierarchical approaches- multi commodity flow based techniques- Randomized Routing- One Step approach- Integer Linear Programming .Detailed Routing: Channel Routing- Switch box routing.

Routing in FPGA: Array based FPGA- Row based FPGAs .

**UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT**

9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing –

Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming

Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock

Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization.

**UNIT V SINGLE LAYER ROUTING CELL GENERATION AND COMPACTION**

9

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing- Multiple chip modules(MCM)- Programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, McGraw Hill International Edition 1995.
- 2 Preas M. Lorenzatti, “ Physical Design and Automation of VLSI systems”, The Benjamin Cummins Publishers, 1998.
- 3 Wayne Wolf, “Modern VLSI Design System – On-chip Design”, Pearson Education First Indian Reprint 2002.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the basic concepts of gate array with algorithm paradigms
- CO2** Infer the methods of placement and partitioning using various algorithms
- CO3** Understand the fundamental routing techniques used in FPGA design
- CO4** Estimate various performance metrics in FPGA circuit layout
- CO5** Familiarize the concepts of circuit compaction in PLA

**16VL712 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS L T P C**

**3 0 0 3**

**UNIT-I SINGLE STAGE AMPLIFIERS 9**

Common source stage- Source follower- Common gate stage-Cascode stage- Single ended and differential operation- Basic differential pair -Differential pair with MOS loads.

**UNIT-II BIASING CIRCUITS 9**

Basic current mirrors, cascode current mirrors, active current mirrors voltage references, supply independent biasing- temperature independent references-PTAT current generation- Constant-Gm Biasing.

**UNIT-III FREQUENCY RESPONSE AND NOISE ANALYSIS 9**

Miller effect, Association of poles with nodes-frequency response of common source stage- Source followers-Common gate stage, Cascode stage, Differential pair-Statistical characteristics of noise-, noise in single stage amplifiers, noise in differential amplifiers.

**UNIT-IV OPERATIONAL AMPLIFIERS 9**

Concept of negative feedback- Effect of loading in feedback networks operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps- Input range limitations- Gain boosting- slew rate power supply rejection- noise in Op Amps.

**UNIT-V STABILITY AND FREQUENCY COMPENSATION 9**

General considerations- Multipole systems - Phase Margin - Frequency Compensation- Compensation of two stage Op Amps- Slewing in two stage Op Amps- Other compensation techniques.

**L : 45 T: 0 P: 0 Total: 45 PERIODS**

**REFERENCES**

- 1 Behzad Razavi, —Design of Analog CMOS Integrated Circuits, Tata McGraw Hill, 2001
- 2 Willey M.C. Sansen, —Analog design essentials, Springer, 2006.
- 3 Grebene, —Bipolar and MOS Analog Integrated circuit design, John Wiley & sons, Inc., 2003.
- 4 Phillip E. Allen, Douglas R. Holberg, —CMOS Analog Circuit Design, Second Edition, Oxford University Press, 2002
- 5 A. Johns and Kenneth W. Martin, Tony Chan Carusone, David, Analog Integrated Circuit Design Wiley 2011

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the concepts of single stage amplifier used in analog IC design
- CO2** Familiarize the reference voltage biasing and current mirror circuits
- CO3** Estimate the frequency response and noise analysis of single stage amplifiers
- CO4** Analyze the performance of single and multistage opamps for IC design
- CO5** Evaluate the stability and frequency compensation of Analog IC design



**UNIT-I VLSI AND ITS ALLIED FIELD****9**

Introduction to Active Filters (PLL) & Switched capacitor filters Active RC Filters for monolithic filter design: First & Second order filter realizations - universal active filter (KHN) - self tuned filter - programmable filters - Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample & hold circuits – Integrator- Biquad.

**UNIT-II CONTINUOUS TIME FILTERS& DIGITAL FILTERS****9**

Introduction to Gm - C filters - bipolar transconductors - CMOS Transconductors using Triode transistors, active transistors – BiCMOS transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance - Digital Filters: Sampling – decimation – interpolation - implementation of FIR and IIR filters.

**UNIT-III DIGITAL TO ANALOG & ANALOG TO DIGITAL CONVERTERS****9**

Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's. Sigma Delta Converters: Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's.

**UNIT-IV ANALOG AND MIXED SIGNAL EXTENSIONS TO VHDL****9**

Introduction - Language design objectives - Theory of differential algebraic equations - the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples.

**UNIT-V ANALOG EXTENSIONS TO VERILOG****9**

Introduction –data types –Expressions-Signals-Analog Behavior-Hierarchical structures-Mixed Signal Interaction. Introduction - Equation construction - solution - waveform Filter functions - simulator - Control Analysis - Multi -disciplinary model.

**L : 45 T : 0 P : 0 Total: 45 PERIODS****REFERENCES**

- 1 David A. Johns, Ken Martin, "Analog Integrated Circuit Design" John Wiley & Sons, 2002.
- 2 Rudy van de Plassche "Integrated Analog-to-Digital and Digital-to-Analog Converters", Kluwer 1999.
- 3 Antoniou, "Digital Filters Analysis and Design" Tata McGraw Hill, 1998.
- 4 Phillip Allen and Douglas Holmberg "CMOS Analog Circuit Design" Oxford University. Press, 2000.
- 5 BenhardRazavi, "Data Converters", Kluwer Publishers, 1999.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the concepts of active and programmable filters in mixed signal circuits
- CO2** Familiarize the digital and continuous time filters used in mixed signal circuits
- CO3** Infer the need of ADC/DAC in mixed signal circuits to improve linearity
- CO4** Relate the techniques used for analog and mixed signal extensions to VHDL
- CO5** Relate the techniques used for analog and mixed signal extensions verilog



**UNIT I POWER DISSIPATION IN CMOS****9**

Sources of power Dissipation–Physics of power dissipation in MOSFET devices, Power dissipation in CMOS, Low power VLSI design limits.

**UNIT II LOW POWER ADDERS AND MULTIPLIERS****9**

Standard adder cells, CMOS adder architectures, BiCMOS adder, overview and types of Multipliers- Braun Multiplier, Baugh – Wooley Multiplier, Wallace Tree Multiplier, Booth Multiplier

**UNIT III SYNTHESIS FOR LOW POWER****9**

Behavioral level transforms-Algorithm using First –Order, second, M<sup>th</sup> Order Differences-Parallel Implementation Pipelined Implementation- Logic level optimization– Technology dependent and Independent– -Circuit level- Static, Dynamic, PTL,DCVSL,PPL

**UNIT IV LOW POWER STATIC RAM ARCHITECTURES****9**

Organization of a static RAM, MOS static RAM memory cell, Banked organization of SRAMs, Reducing voltage swings on bit lines, Reducing power in the write driver circuits, Reducing power in sense amplifier circuits.

**UNIT V LOW ENERGY COMPUTING USING ENERGY RECOVERY TECHNIQUES****9**

Energy dissipation in transistor channel using an RC model, Energy recovery circuit design, Designs with partially reversible logic, Supply clock generation.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 K.Roy and S.C. Prasad, Low Power CMOS VLSI Circuit Design, Wiley, 2000.
- 2 K.S. Yeo and K.Roy, Low-Voltage, Low-Power VLSI Subsystems, Tata McGraw-Hill, 2004.
- 3 Dimitrios Soudris, Chirstian Pignet and Costas Goutis, Designing CMOS Circuits for Low Power, Kluwer, 2009.
- 4 James B. Kuo and Shin – Chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits, John Wiley and Sons, 2001.
- 5 J.B Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley, 1999.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the fundamental concepts power dissipation in CMOS
- CO2** Infer the types of low power adder and multipliers for circuit optimization techniques
- CO3** Evaluate the different types of algorithm in low poer synthesis
- CO4** Analyze the low power static ram architecture design in power efficient design
- CO5** Familiarize the techniques and process used to low energy computing

**UNIT-I MEMS AND MICROSYSTEMS**

MEMS and Microsystems products, evaluation of micro fabrication, micro-systems and microelectronics, applications of Microsystems, working principles of Microsystems, micro-sensors, micro-actuators, MEMS and micro-actuators, micro-accelerometers. Scaling Laws In Miniaturization: Introduction, scaling in geometry, scaling in rigid body dynamics, the trimmer force scaling vector, scaling in electrostatic forces.

**UNIT-II MATERIALS FOR MEMS AND MICROSYSTEMS**

9

Substrates and wafers, silicon as a substrate material, ideal substrates for MEMS, single crystal silicon and wafers crystal structure, mechanical properties of Si, silicon compounds, SiO<sub>2</sub>, SiC, Si<sub>3</sub>N<sub>4</sub>. And polycrystalline Silicon, silicon piezo resistors, gallium arsenide, quartz, piezoelectric crystals, polymers for MEMS, conductive polymers.

**UNIT-III ENGINEERING MECHANICS FOR MICROSYSTEMS DESIGN**

9

Introduction, static bending of thin plates, circular plates with edge fixed rectangular plate with all edges fixed and square plates with all edges fixed. Mechanical vibration, resonant vibration, micro accelerometers, design theory d damping coefficients. Thermo mechanics, thermal stresses. Fracture mechanics, stress intensity factors, fracture toughness and interfacial fracture machine.

**UNIT-IV BASICS OF FLUID MECHANICS IN MACRO AND MESO SCALES**

9

Viscosity of fluids, flow patterns Reynolds number. Basic equation in continuum fluid dynamics, laminar fluid flow in circular conduits, computational fluid dynamics, and incompressible fluid flow in micro conducts surface tension, capillary effect and micro pumping. Fluid flow in sub micrometer and nanoscale, rare field gas, kundsens and Mach number and modeling of micro gas flow, heat conduction in multilayered thin films.

**UNIT-V MICROSYSTEM FABRICATION PROCESS**

9

Photolithography, photo resist and applications, light sources. Ion implantation, diffusion process, oxidation, thermal oxidation, silicon diode, thermal oxidation rates, Oxide thickness by colour. Chemical vapour deposition, principle, reactants in CVD, enhanced CVD physical vapour defusing, sputtering, deposition by epitaxial etching, chemical and plasma etching.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 Tai-Ran Hus, MEMS and Microsystems Design and Manufacture, Tata McGraw-Hill, 2001.
- 2 John A Pelesko, Modeling MEMs and NEMS, CRC Press, 2002.
- 3 Chang Liu, Foundation of MEMS, Pearson Edition, 2005
- 4 Stephen Beeby, Graham Ensell, MEMS, Mechanical Sensors, Artech House Publishers, 2004.
- 5 Wanjun Wang, Steven A. Soper, Bio-MEMS Technologies and Applications, CRC Press, 2007.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the fundamental concepts and working principles of MEMS and Microsystems
- CO2** Infer the types of material used to design MEMS and microsystem devices
- CO3** Analyze the physical and mechanical characteristics of MEMS devices
- CO4** Evaluate the fluid mechanics of MEMS devices in macro and meso scales
- CO5** Familiarize the techniques and process used to fabricate MEMS devices

**UNIT-I THE BLUETOOTH MODULE****9**

Introduction-overview - the Bluetooth module-antennas-baseband-introduction-Bluetooth device address – masters, slaves, and Pico nets-system timing-physical links-Bluetooth packet structure-logical channels frequency hopping.

**UNIT-II THE LINK CONTROLLER****9**

The link controller-link control protocol-link controller operation-Pico net, scatter net operation master/slave role switching-base band/link controller architectural overview -link manager-the host controller interface.

**UNIT-III THE BLUE TOOTH HOST****9**

The blue tooth host-logical link control and adaptation protocol –RFCOMM- the service discovery protocol –the wireless access protocol-OBEX and IrDA-telephony control protocol.

**UNIT-IV CROSS LAYER FUNCTIONS****9**

Cross layer functions-Encryption and security-low power operations-controlling low power modes-hold mode sniff mode-park mode-quality of service-managing Bluetooth devices.

**UNIT-V TEST AND QUALIFICATION****9**

Test and qualification- test mode-qualification and type approval-implementation – related standards and technologies.

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 Jennifer Bray, Brain Senese, Gordon McNutt, Bill Munday, “ Bluetooth Application Developer’s Guide”, Syngress Media, 2001.
- 2 Micheal Mille,” Discovering Bluetooth”.
- 3 C S R Prabhu, P A Reddi, “ Bluetooth Technology and its applications with JAVA and J2ME”, PHI ,2006

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Identify the types of Bluetooth module and frequency hopping techniques
- CO2** Understand the principles and performance of link controller .
- CO3** Infer the performance of Bluetooth host
- CO4** Familiarize the cross layer functions in Bluetooth devices
- CO5** Apply the test and qualification techniques in Bluetooth technology

**UNIT-I MULTIPROCESSORS AND SCALABILITY ISSUES****9**

Scalable design principles – Principles of processor design – Instruction Level Parallelism, Thread level parallelism - Parallel computer models –Symmetric and distributed shared memory architectures – Performance Issues – Multi-core Architectures - Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture – SUN CMP architecture.

**UNIT-II MULTICORE SYSTEMS ON-CHIP****9**

MCSoc Design Problems – SoC typical architecture- Multicore architecture Platform – Application specific MCSoc design method, Queue Core architecture: synthesis and evaluation, Network-on-Chip –Router Architecture, Topology, Routing

**UNIT-III LOW POWER AND RECONFIGURABLE CORES****9**

Low Power Embedded QC2 Core - Architecture, Synthesis, Design Approach, Reconfigurable Multicore – Performance, Power Aware technological level optimizations - Power Aware system design optimizations - Hardware Adaptation, Software Adaptation, Future Directions

**UNIT-IV PARALLEL PROGRAMMING****9**

Fundamental concepts – Designing for threads – Scheduling -Threading and parallel programming constructs – Synchronization –Critical sections – Deadlock. Threading APIs

**UNIT-V MULTITHREADED APPLICATION DEVELOPMENT****9**

Multithreaded Applications – Algorithms – Dynamic Multithreading -Analysis of Multithreaded Algorithms, Parallel Loops, Race Condition -Performance measures - Program development and performance tuning

**L : 45****T: 0****P: 0****Total: 45 PERIODS****REFERENCES**

- 1 ShameemAkhter and Jason Roberts, Multi-core Programming, Intel Press, First Edition, 2006.
- 2 Ben AbadallahAbderazek, Multicore Systems On-Chip : PracticalSoftware Hardware Design, Atlantis Press, Second Edition, 2010
- 3 Michael J Quinn, Parallel programming in C with MPI and Open MP, Tata McGraw Hill, First Edition, 2003.
- 4 John L. Hennessy and David A. Patterson,Computerarchitecture,A quantitative approach, Morgan Kaufmann Elsevier Publishers, Fourth Edition, 2007.
- 5 David E. Culler and Jaswinder Pal Singh,Parallel computing architecture: A hardware software approach, Morgan Kaufmann/Elsevier Publishers, First Edition, 1999

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Identify the types of multiprocessors based on applications and its performance issues
- CO2** Understand the principles and performance of Multicore soc architecture.
- CO3** Infer the low power multi core processors and its optimization techniques
- CO4** Familiarize the fundamental concepts of parallel processing
- CO5** Apply the algorithms in multithreaded applications to improve the performance of multicore Processors.

**UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9**

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. Basic CMOS technology

**UNIT II INVERTERS CIRCUIT ANALYSIS 9**

NMOS Inverters, Stick diagram, Inverter ratio, DC characteristics, Transient characteristics, Switching times, Super buffers, Driving large capacitance loads.

**UNIT III CMOS LOGIC GATES 9**

CMOS Inverters, CMOS logic structures, Transmission gates, Static CMOS design, dynamic CMOS design.

**UNIT IV CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9**

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation, Charge sharing.

**UNIT V VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9**

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits– Ripple carry adders, Carry look ahead adders, Multipliers, Physical design – Delay modeling, floor planning.

**L : 45 T: 0 P: 0 Total: 45 PERIODS**

**REFERENCES**

- 1 John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
- 2 Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 2002.
- 3 Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2002.
- 4 Stephen Brown, Zvonko Vranesic, "Fundamentals of Digital Logic Design With VHDL", Second Edition 2007.
- 5 Kamran, Eshraghian, Douglas A. Pucknell, Sholeh Eshkaghien, "Essentials of VLSI Circuits and Systems", PHI Publications, 2005.

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** Understand the basic concepts of MOS transistor theory and its process technology
- CO2** Analyze the CMOS inverter transient and switching characteristics
- CO3** Infer the types of CMOS digital logic circuits to design a static and dynamic logic design
- CO4** Estimate the power dissipation and low power performance of VLSI circuits
- CO5** Model a system component of VLSI circuits in physical layer of abstraction

**UNIT I INTRODUCTION OF IoT****9**

Definition & Characteristics of IoT - Challenges and Issues - Physical Design of IoT, Logical Design of IoT - IoT Functional Blocks, Security

**UNIT II PROTOCOLS OF IoT****9**

Control Units – Communication modules – Bluetooth – Zigbee – Wifi – GPS- IOT Protocols (IPv6, 6LoWPAN, RPL, CoAP etc.), MQTT, Wired Communication, Power Sources.

**UNIT III PILLARS OF IoT****9**

Four pillars of IOT paradigm, - RFID, Wireless Sensor Networks, SCADA (Supervisory Control and Data Acquisition), M2M - IOT Enabling Technologies - BigData Analytics, Cloud Computing, Embedded Systems.

**UNIT IV WEB OF THINGS****9**

Clustering, Clustering for Scalability, Clustering Protocols for IOT. The Future Web of Things – Set up cloud environment – Cloud access from sensors – Data Analytics for IOT- Case studies- Open Source 'e-Health sensor platform' – 'Be Close Elderly monitoring' – Other recent projects.

**UNIT V APPLICATIONS OF IoT****9**

Working principles of sensors – IOT deployment for Raspberry Pi /Arduino/Equivalent platform – Reading from Sensors, Communication: Connecting microcontroller with mobile devices – communication through Bluetooth, wifi and USB - ContikiOS Cooja Simulator.

**L : 45 T: 0 P: 0 Total: 45 PERIODS****REFERENCES**

- 1 Dieter Uckelmann et.al, "Architecting the Internet of Things", Springer, 2011
- 2 Arshdeep Bahga and Vijay Madisetti, "Internet of Things – A Hand-on Approach", Universities press, 2015.
- 3 Charalampos Doukas, "Building Internet of Things with the Arduino", Create space, April 2002
- 4 Dr. Ovidiu Vermesan and Dr. Peter Friess, "Internet of Things: From research and innovation to market deployment", River Publishers 2014
- 5 Contiki : The open source for IOT, [www.contiki-os.org](http://www.contiki-os.org)

**COURSE OUTCOMES**

At the end of the course student should be able to:

- CO1** understand the fundamental concepts of communication models and protocols in IoT
- CO2** relate the protocols used in wired and wireless mode of communication in IoT
- CO3** analyze the working principles of four pillars of IoT with real time applications
- CO4** Familiarize the concepts of Web of things and clustering protocols for communication.
- CO5** infer the principles of sensors and communication protocols used in IoT devices